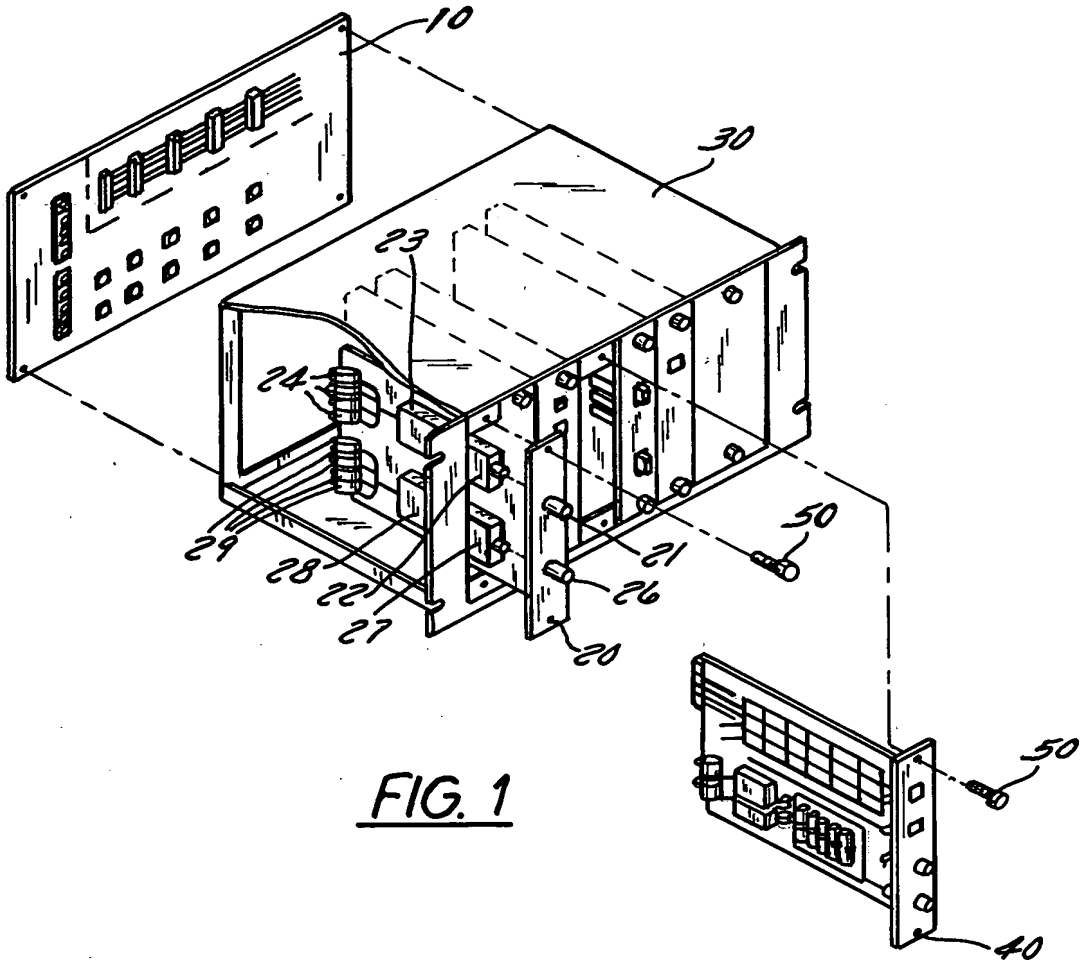
10
30
23
24
29
28
22
27
21
26
20
50
50
40

FIG. 1

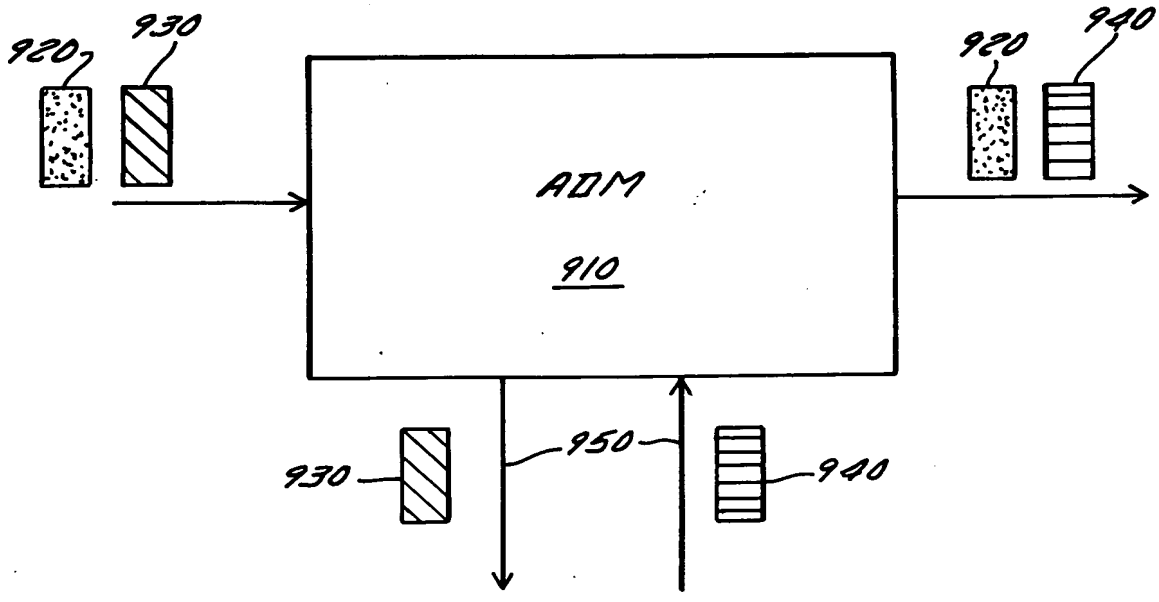
920
930
ADM
910
920
940
930
950
940

FIG. 9

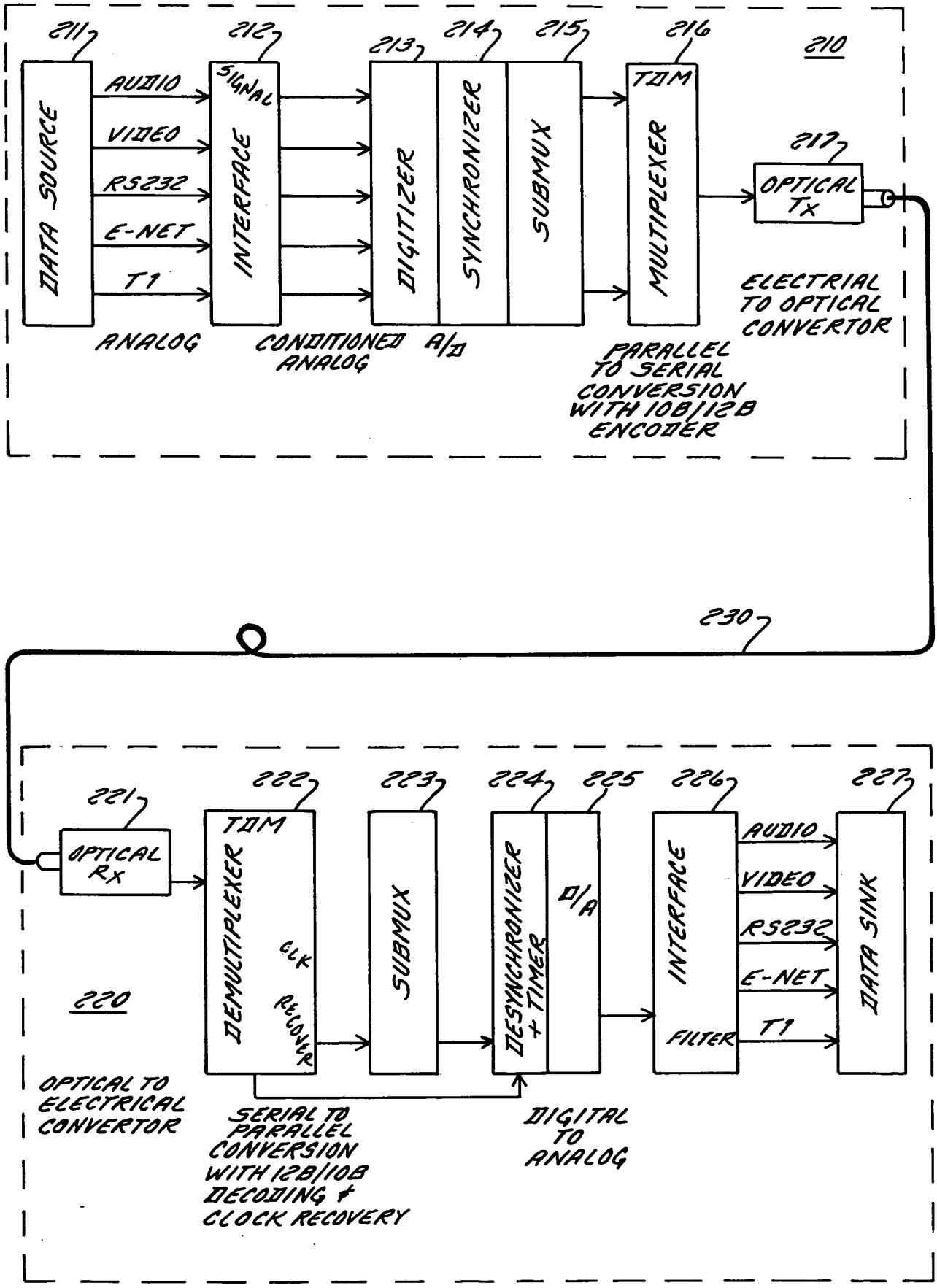
211
212
213
214
215
216
210
DATA SOURCE
AUDIO
VIDEO
RS232
E-NET
T1
SIGNAL INTERFACE
DIGITIZER
SYNCHRONIZER
SUBMUX
TDM MULTIPLEXER
217
OPTICAL Tx
ELECTRIAL TO OPTICAL CONVERTOR
ANALOG
CONDITIONED ANALOG
A/D
PARALLEL TO SERIAL CONVERSION WITH 10B/12B ENCODER
230
221
222
223
224
225
226
227
OPTICAL Rx
TDM DEMULTIPLEXER
CLK RECOVER
SUBMUX
DESYNCHRONIZER + TIMER
D/A
INTERFACE
FILTER
AUDIO
VIDEO
RS232
E-NET
T1
DATA SINK
220
OPTICAL TO ELECTRICAL CONVERTOR
SERIAL TO PARALLEL CONVERSION WITH 12B/10B DECODING + CLOCK RECOVERY
DIGITAL TO ANALOG

FIG. 2

T09030 "0262260

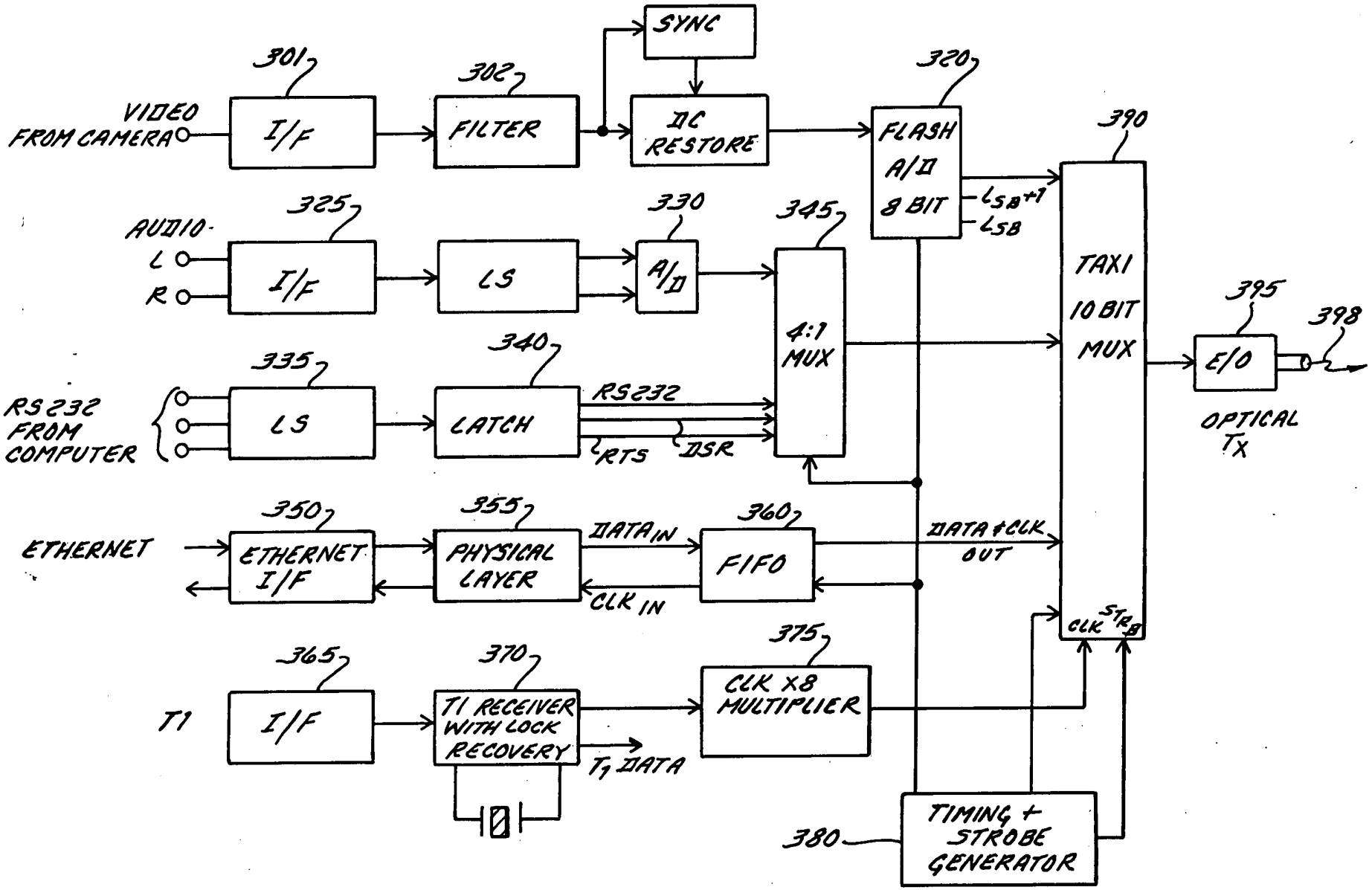

FIG. 3

T09030 "02627260

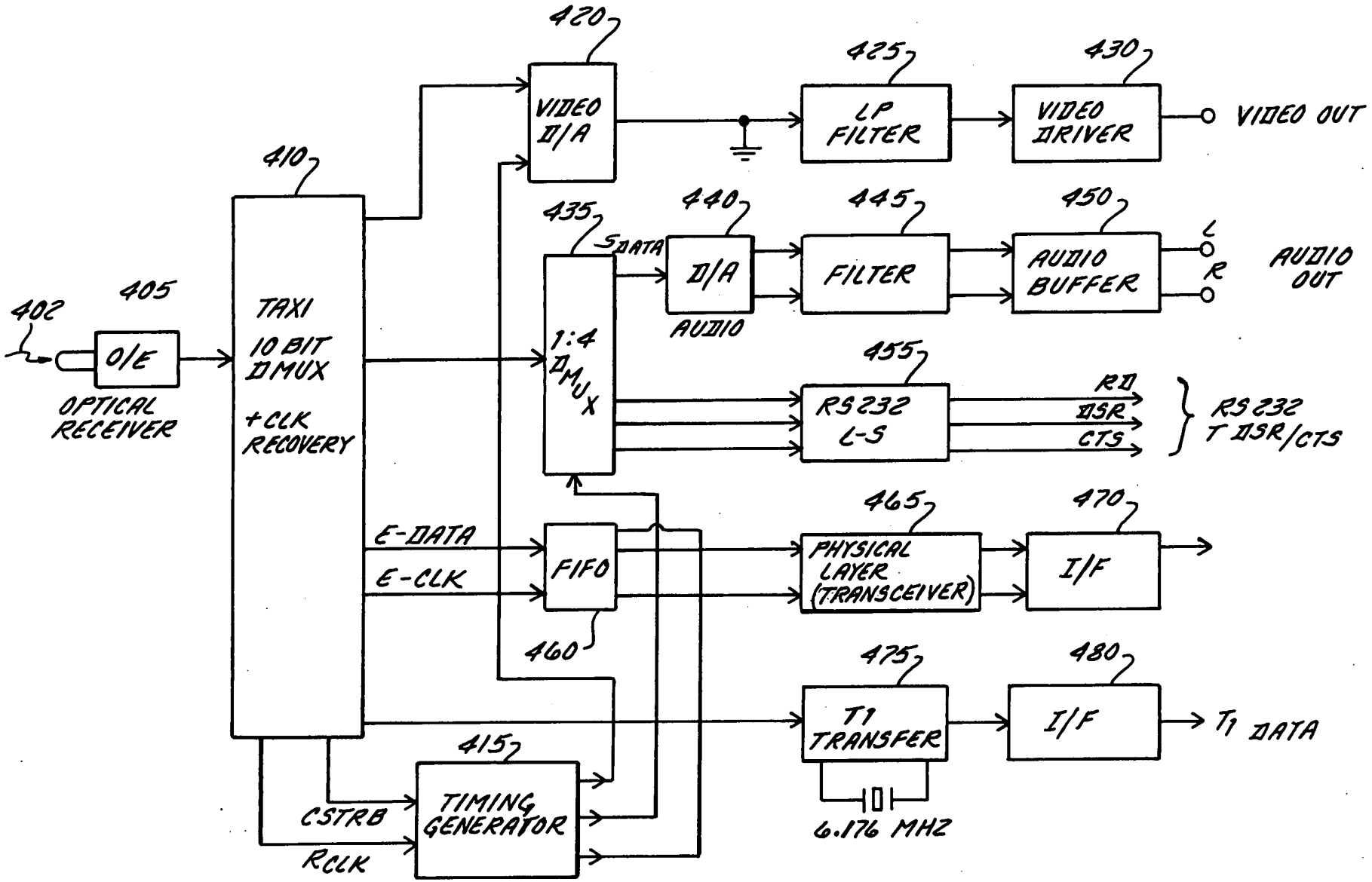

FIG. 4

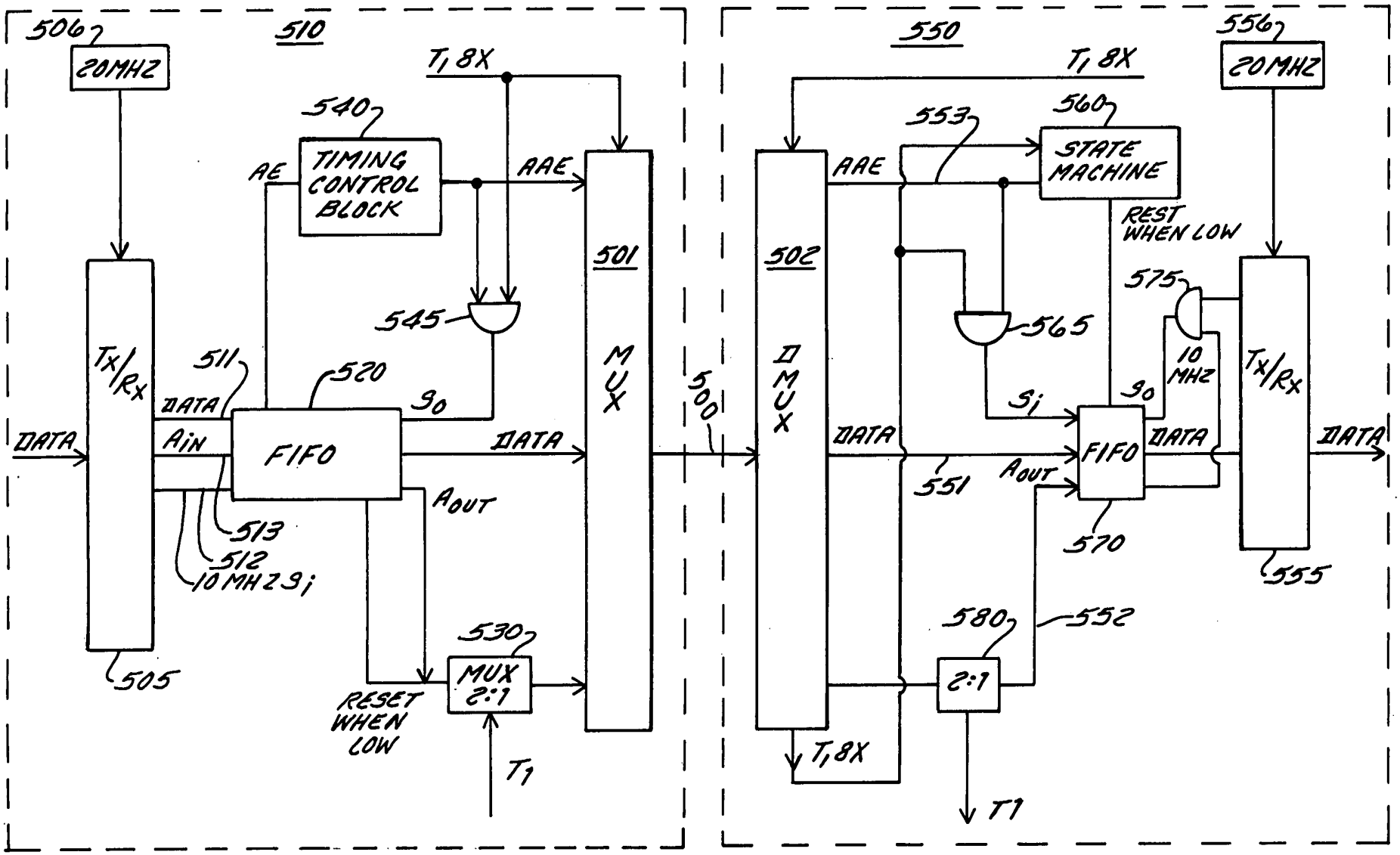
506
20MHZ
510
T1 8X
540
TIMING CONTROL BLOCK
AE
AAE
545
501
MUX
500
511
520
90
DATA
AIN
FIFO
DATA
AOUT
513
512
10MHZ Sj
505
530
MUX 2:1
RESET WHEN LOW
T1
550
T1 8X
553
560
STATE MACHINE
AAE
REST WHEN LOW
502
DMUX
565
575
10 MHZ
Sj
90
DATA
FIFO
DATA
AOUT
551
570
556
20MHZ
TX/RX
555
DATA
580
552
2:1
T1 8X
T1

FIG. 5

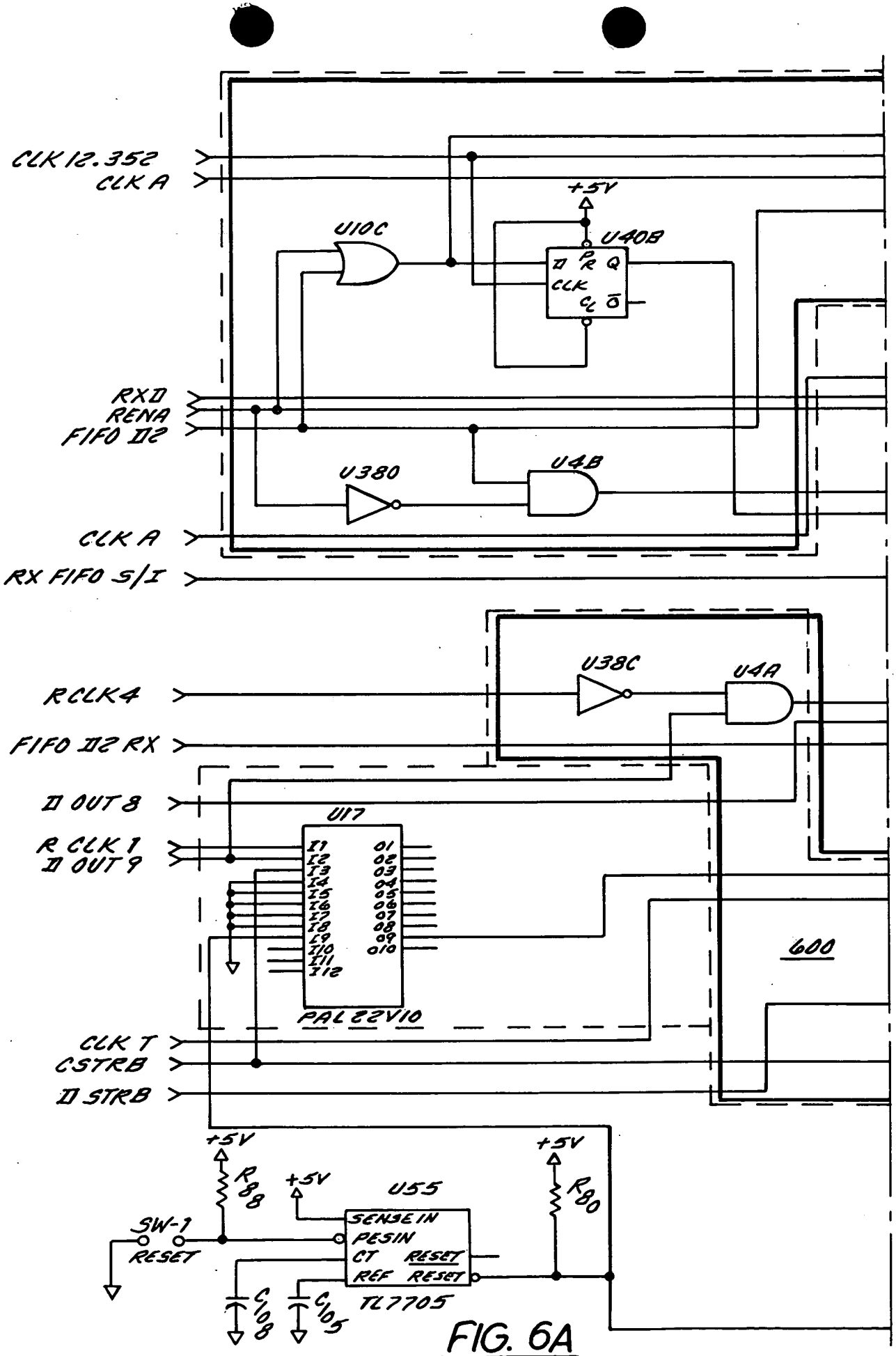
CLK 12.352
CLK A
+5V
U10C
U40B
D PR Q
CLK
CL Q
RXD
RENA
FIFO D2
U38D
U4B
CLK A
RX FIFO S/I
U38C
U4A
RCLK4
FIFO D2 RX
D OUT 8
U17
R CLK 1
D OUT 9
I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12
O1 O2 O3 O4 O5 O6 O7 O8 O9 O10
PAL22V10
600
CLK T
CSTRB
D STRB
+5V
R88
+5V
U55
+5V
R80
SW-1
RESET
SENSE IN
PESIN
CT RESET
REF RESET
C108
C105
TL7705

FIG. 6A

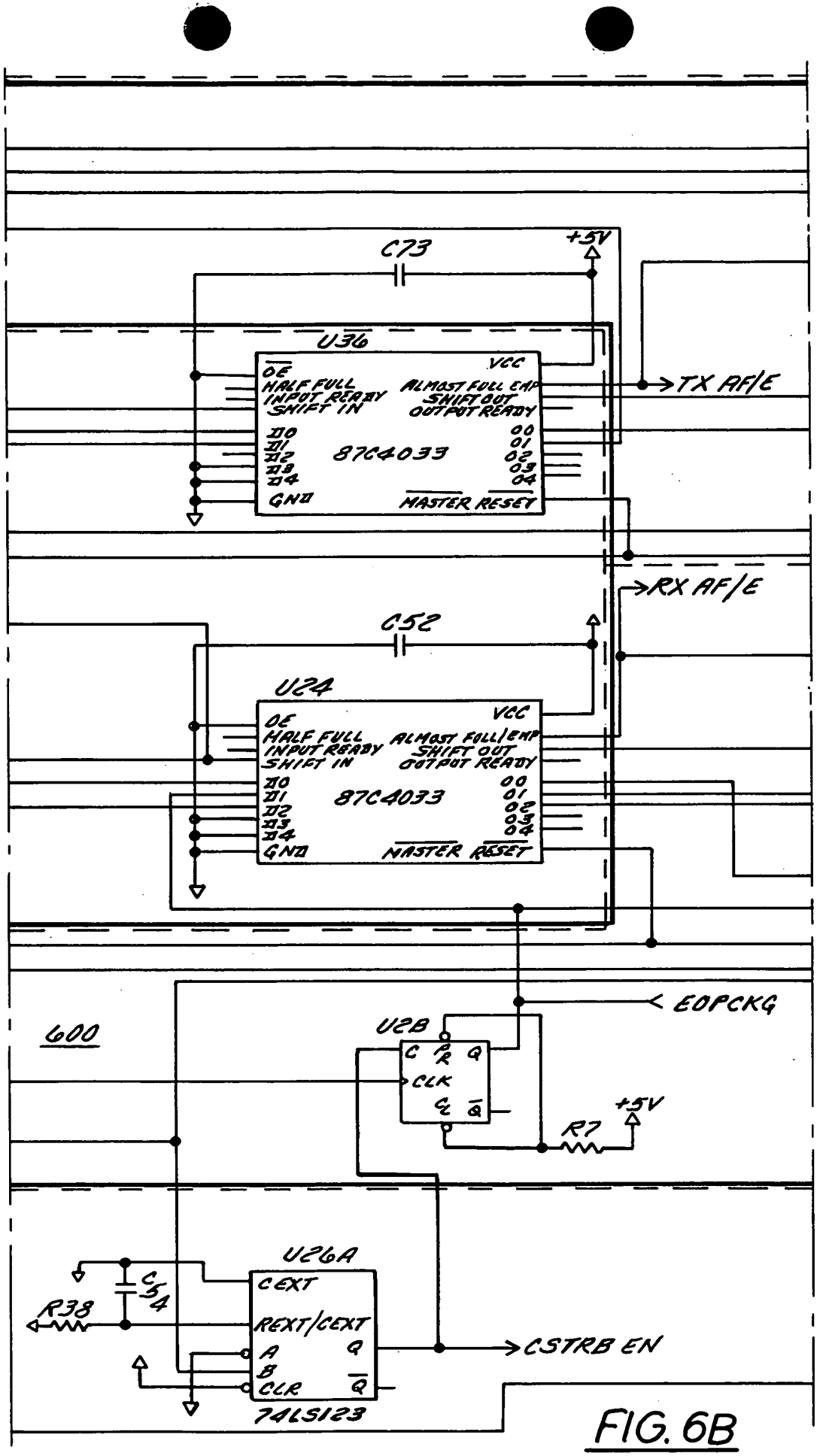
C73
+5V
U36
OE
HALF FULL
INPUT READY
SHIFT IN
VCC
ALMOST FULL/EMP
SHIFT OUT
OUTPUT READY
I0
I1
I2
I3
I4
GND
87C4033
O0
O1
O2
O3
O4
MASTER RESET
TX AF/E
RX AF/E
C52
U24
OE
HALF FULL
INPUT READY
SHIFT IN
VCC
ALMOST FULL/EMP
SHIFT OUT
OUTPUT READY
I0
I1
I2
I3
I4
GND
87C4033
O0
O1
O2
O3
O4
MASTER RESET
EOPCKG
600
U2B
C
PR
Q
CLK
CL
Q
+5V
R7
U26A
C54
R38
CEXT
REXT/CEXT
A
B
CLR
Q
Q
74LS123
CSTRB EN

FIG. 6B

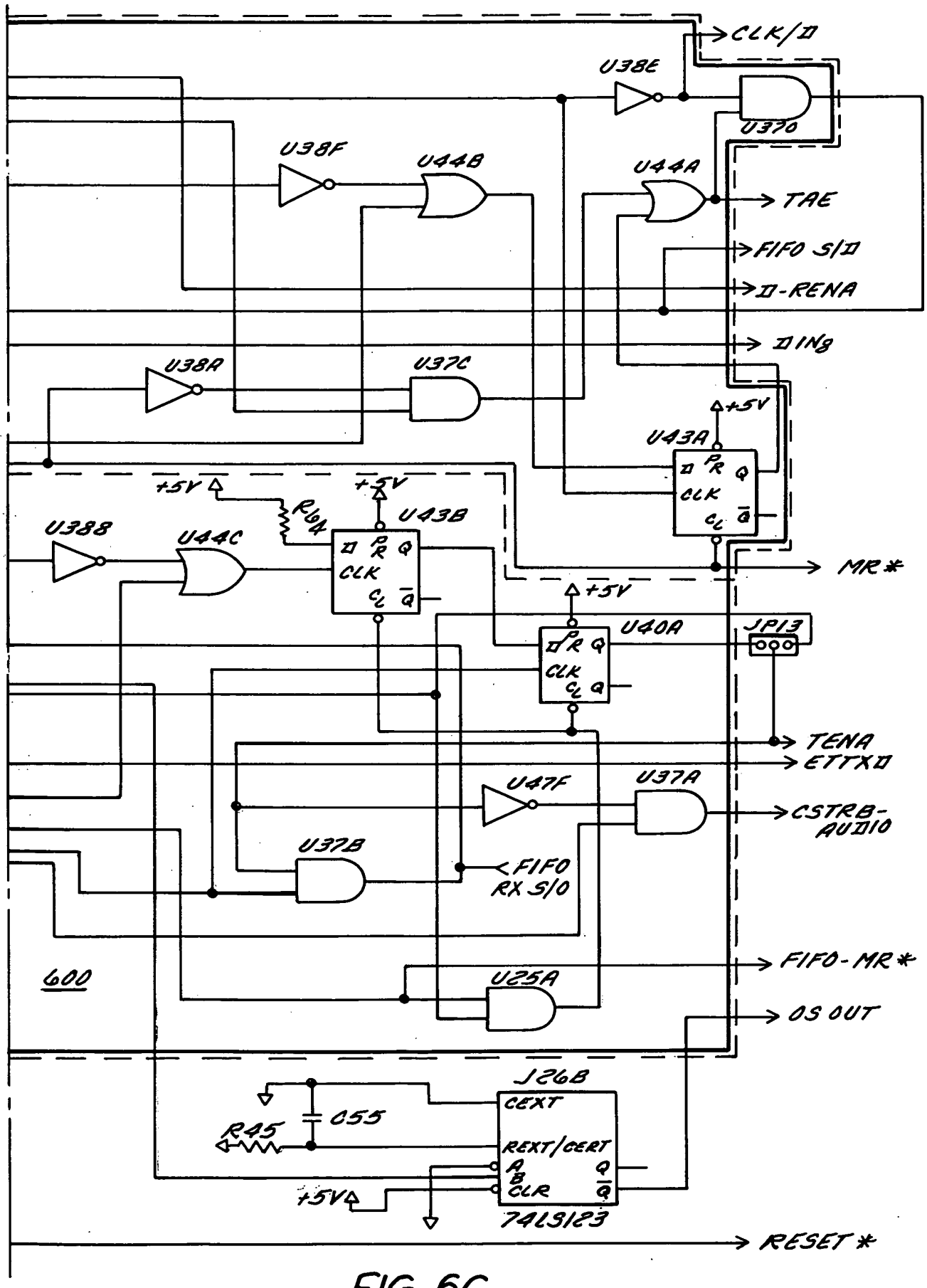
CLK/D
U38E
U37D
U38F
U44B
U44A
TAE
FIFO S/D
D-RENA
D ING
U38A
U37C
+5V
U43A
D PR Q
CLK
CL Q
+5V
+5V
R64
U43B
U38B
U44C
MR*
+5V
U40A
JP13
TENA
ETTXD
U47F
U37A
CSTRB-AUDIO
U37B
FIFO RX S/O
600
FIFO-MR*
U25A
OS OUT
J26B
CEXT
C55
R45
REXT/CEXT
A
B
CLR
Q
Q
+5V
74LS123
RESET*

FIG. 6C

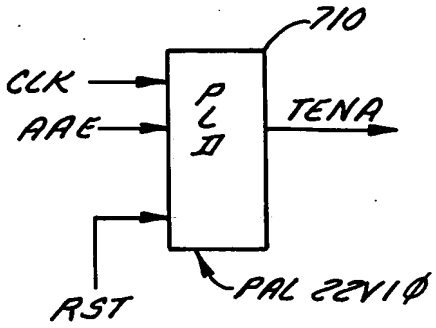
710
CLK
AAE
PAL
TENA
RST
PAL 22V10

FIG. 7A

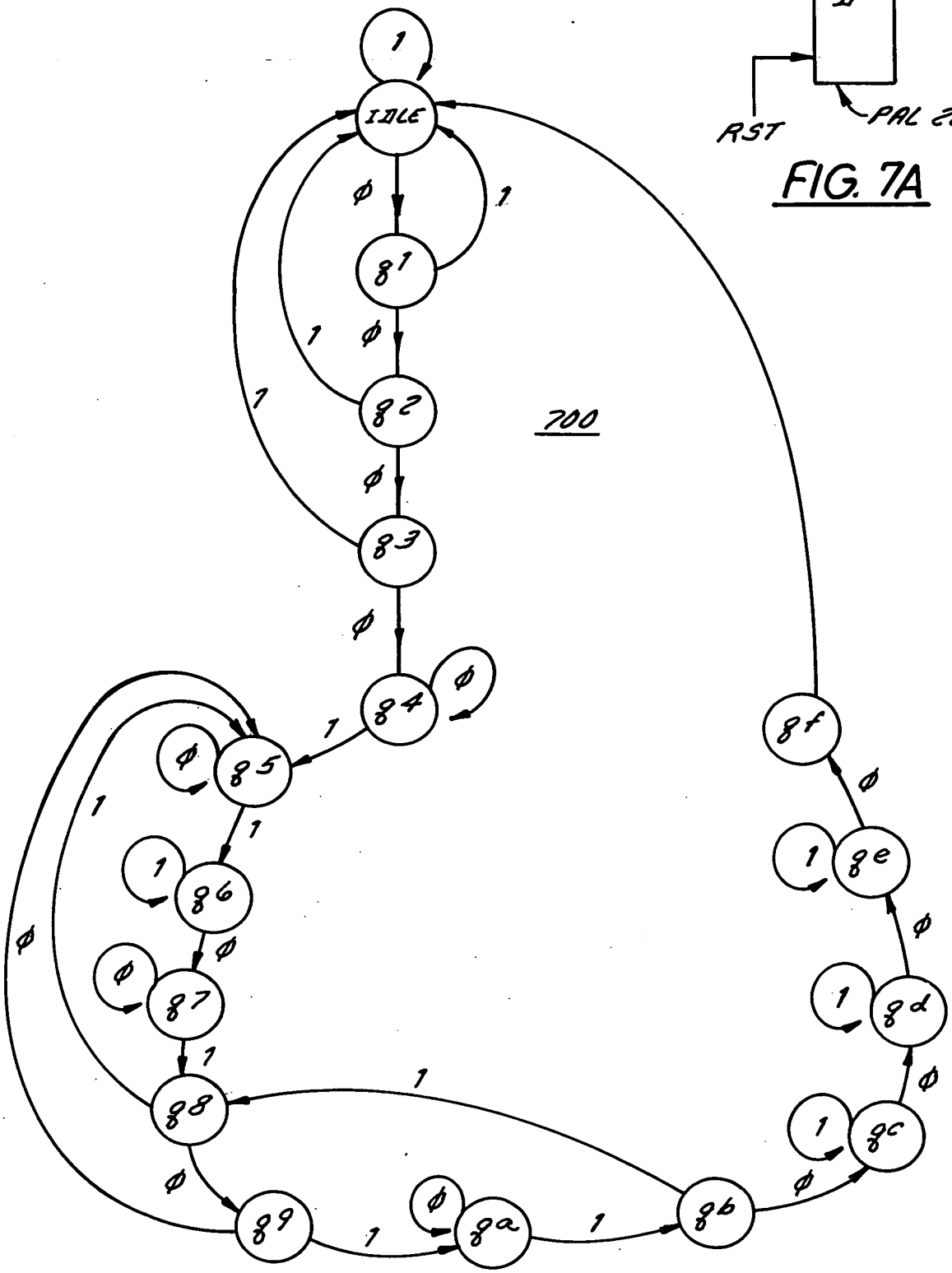
700
IDLE
81
82
83
84
85
86
87
88
89
8a
8b
8c
8d
8e
8f

FIG. 7B

T09030 "0264260

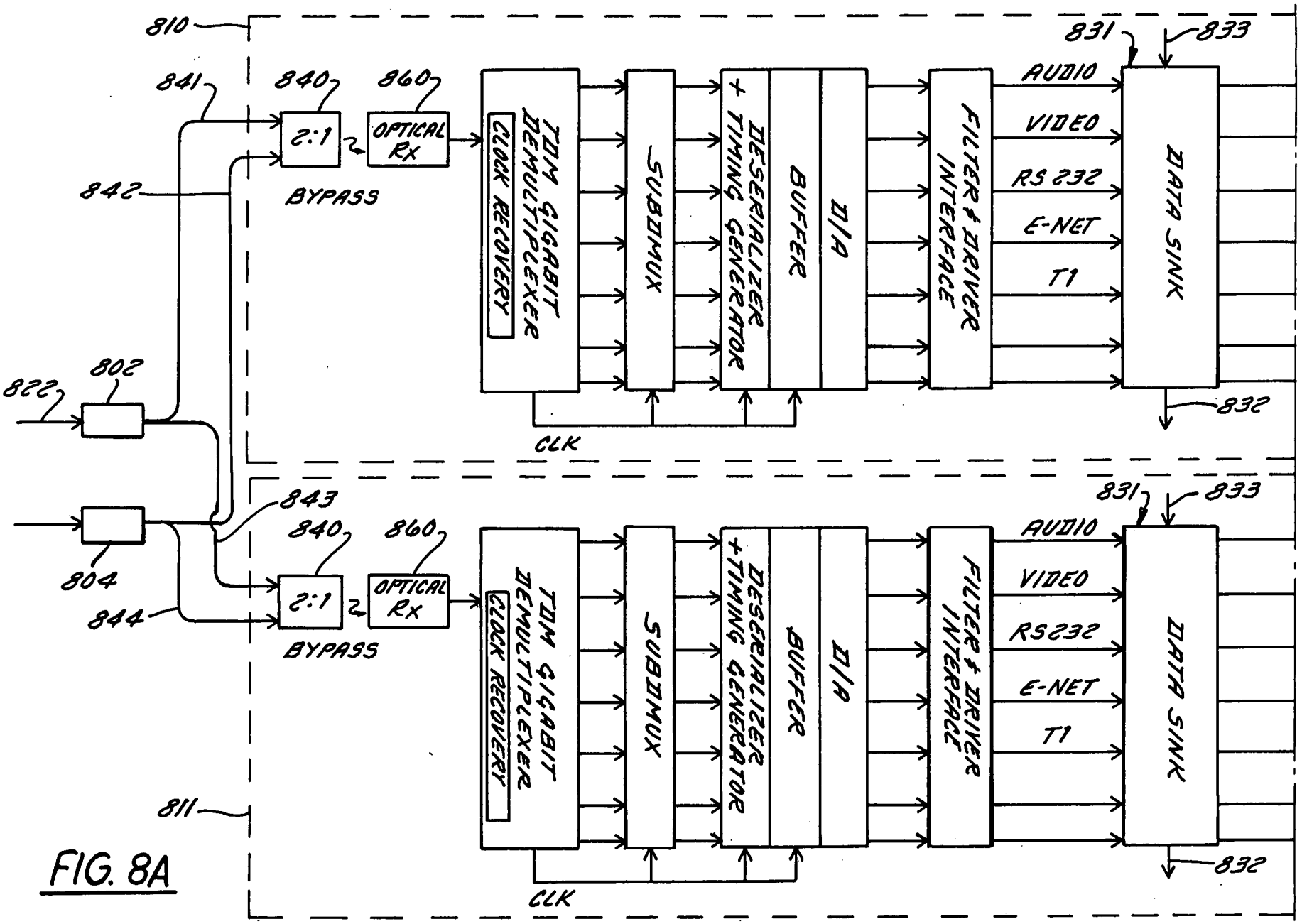

FIG. 8A

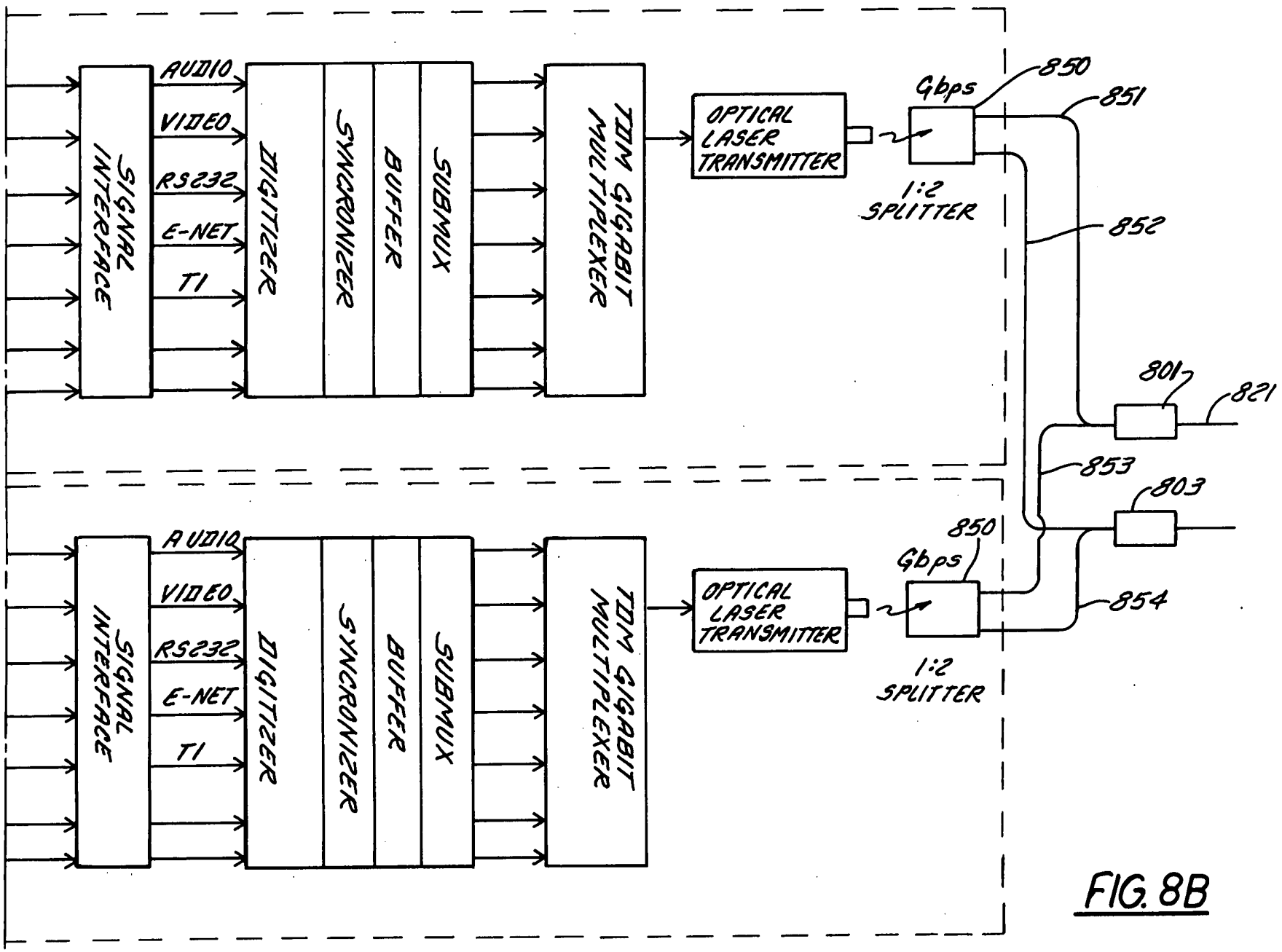
AUDIO
VIDEO
RS232
E-NET
T1
SIGNAL INTERFACE
DIGITIZER
SYNCHRONIZER
BUFFER
SUBMUX
TDM GIGABIT MULTIPLEXER
OPTICAL LASER TRANSMITTER
Gbps
1:2 SPLITTER
850
851
852
853
854
801
803
821

FIG. 8B

TO9030 "0268"2760

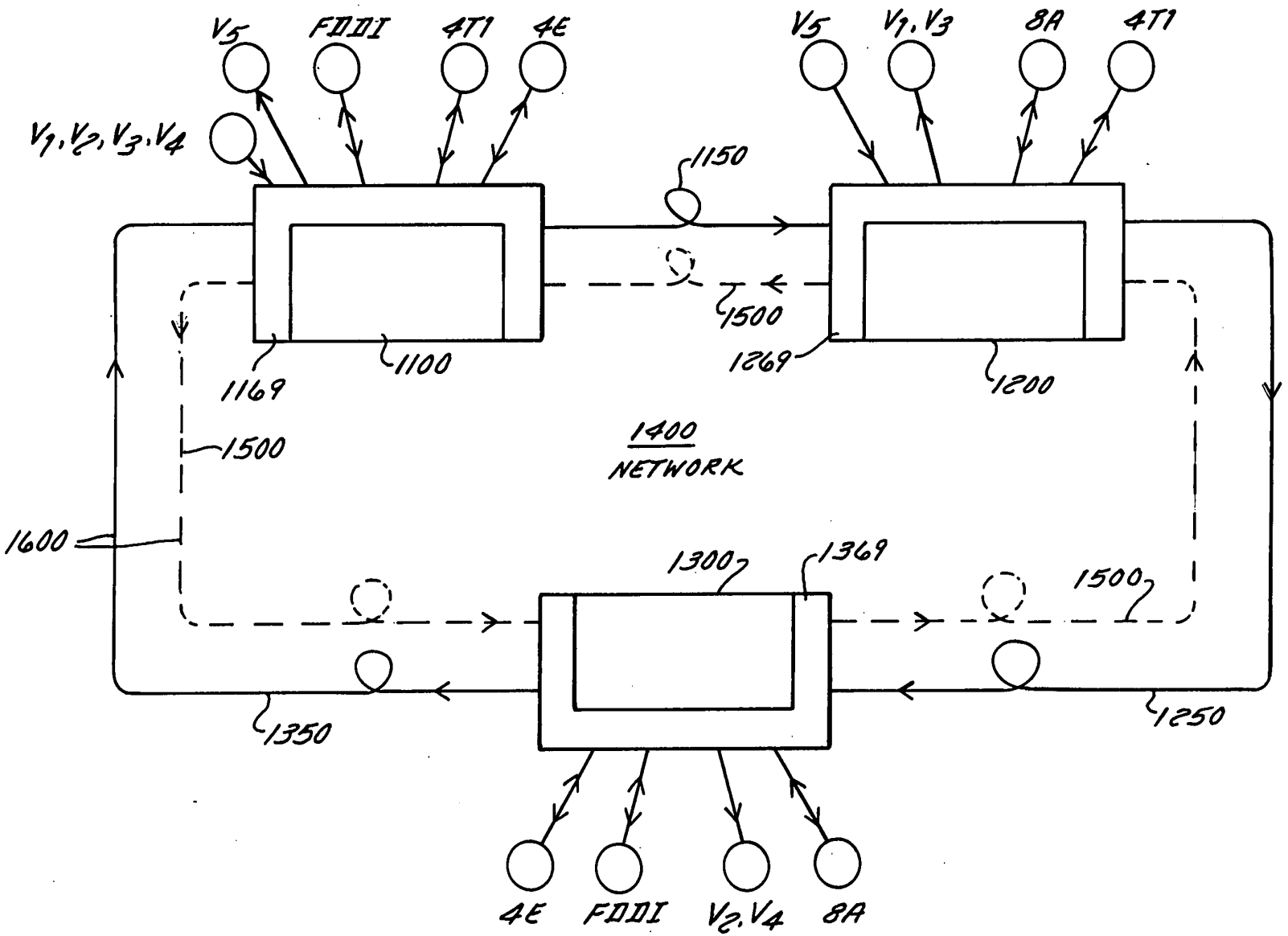

FIG. 10

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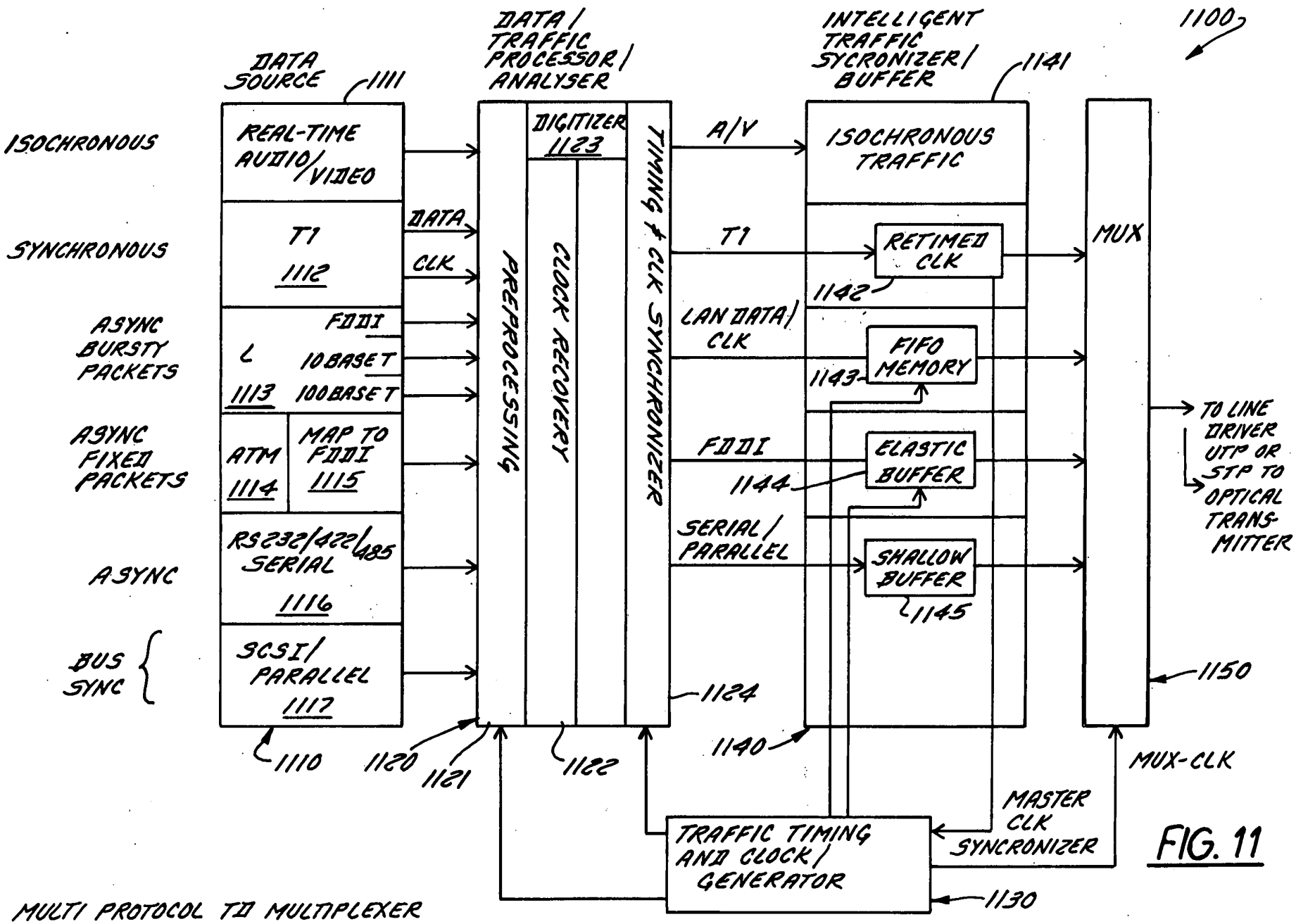

FIG. 11

MULTI PROTOCOL TDM MULTIPLEXER

TD9020 "0762760

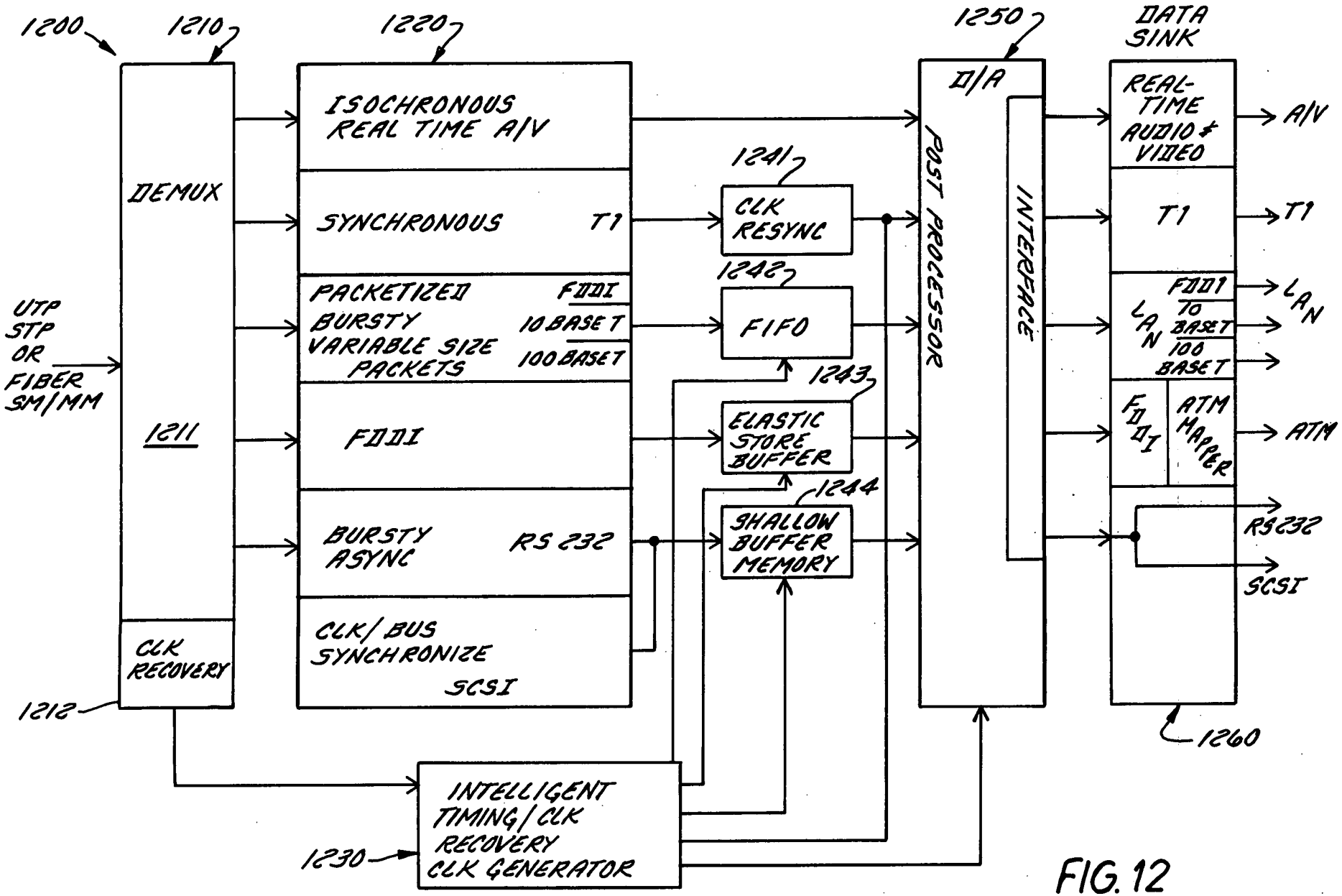

FIG. 12

MULTIPROTOCAL TDM DEMULTIPLEXER

DATA TYPE	MULTIPLEXER/ DEMULTIPLEXER INTERFACE REQUIREMENT	DATA RATE	TIMING SENSITIVITY
AUDIO/ VIDEO MULTIMEDIA	• CONTINUOUS SAMPLING • LOCK MATCHING • MINUMUM BUFFERING	VARIABLE BIT RATE IN COMPRESSED MODE UNCOMPRESSED DEPENDS ON RESOLUTION + SAMPLING RATE	AUDIO/ VIDEO SYNCHRON- IZATION
RS232/422/485 SERIAL ASYNCHRONOUS SCSI PARALLEL BUS SYNCHRONIZED	CAN USE BUFFER OR LOW SPEEDS USE OVERSAMPLING REQUIRE FIFO MEMORY	VARIBLE 10kb/s → 10Mb/s VARIABLE → 40 MBYTE/s	BAUD RATES NEED MATCHING INTERLOCKED HANDSHAKE BUS TIMING SYNCHRON- IZATION
T1	NEED DIRECT MATCHING OF T1 CLK WITH MUX SYNCHRONIZATION OF MASTER CLOCK	1.544 Mb/s	CLOCK/ RECOVERY VERY STRICT TIMING REQUIRE CLK 1.544± 32 PPN
LAN NET- WORK — FDDI	NEED CLOCK RECOVERY MINIMUM BUFFER AND STRICT DATA RATE MATCHING USING SHALLOW FIFO	100 Mb/s	CLOCK RECOVERY REQUIRED ELASTIC BUFFER
LAN NET- WORK — 10 BASE T		10 Mb/s	CLOCK RECOVERY NEEDED
LAN NET- WORK — 100 BASE T		100 Mb/s	CLOCK RECOVERY NEEDED
WIDE AREA ST1/ST3 ATM	PRECISE NEED CLOCK RECOVERY AND DEFRAMING WITH TRANSFER TO PACKET	51.84/155.5 OC1/OC3 Mb/s	TIME/ STAMP REQUIREMENT CLOCK CORRECTION

FIG. 13A

DELAY/LATENCY SENSITIVITY	TRAFFIC TYPE / DATA STREAM	APPLICATIONS	REMARKS TYPE OF CHANNEL
CONSTANT FOR MINIMUM JITTER	CONSTANT BIT RATE LAMINAR BIT STREAM	MULTIMEDIA TELECONFERENCING VIDEO CONFERENCING SECURITY	ISOCHRONOUS
JITTER REQUIREMENT (NOT VERY TIGHT)	VARIABLE BIT RATE	COMPUTER TO COMPUTER / PERIPHERAL COMPUTER TO MEMORY	ASYNCHRONOUS BUS SYNCHRONOUS
MINIMUM JITTER REQUIREMENT FOR VOICE MIN. ACCEPTABLE LATENCY ~ 150 ms	CONSTANT BIT RATE	TELEPHONY WIDE AREA	SYNCHRONOUS
MAX. ELASTICITY FUNCTION OF NETWORK / TOKEN ROTATING TIMES	BURSTY ASYNCHRONOUS PACKETIZED	OPTICAL NETWORK IN BACKBONES	BURSTY PACKETIZED
COLLISSION DOMAIN LIMITED	ASYNCHRONOUS	LAN	ASYCHRONOUS
COLLISSION DOMAIN LIMITED	ASYNCHRONOUS	LAN	ASYCHRONOUS
VARIABLE LATENCY DEPENDING ON TRAFFIC MIN. LATENCY AND JITTER REQUIREMENT FOR VOICE/TELEPHONE AND MULTIMEDIA TRAFFIC	VBR: VARIABLE BIT RATE CBR: CONSTANT BIT RATE ABR: AVAILABLE BIT RATE ASYNCRONOUS TRANSFER MODE ASYNCHRONOUS	WIDE AREA NETWORK	CAN MAP ATM CELLS TO FDDI PACKETS AND THE TRANSFER SYNCHRONOUSLY

FIG. 13B

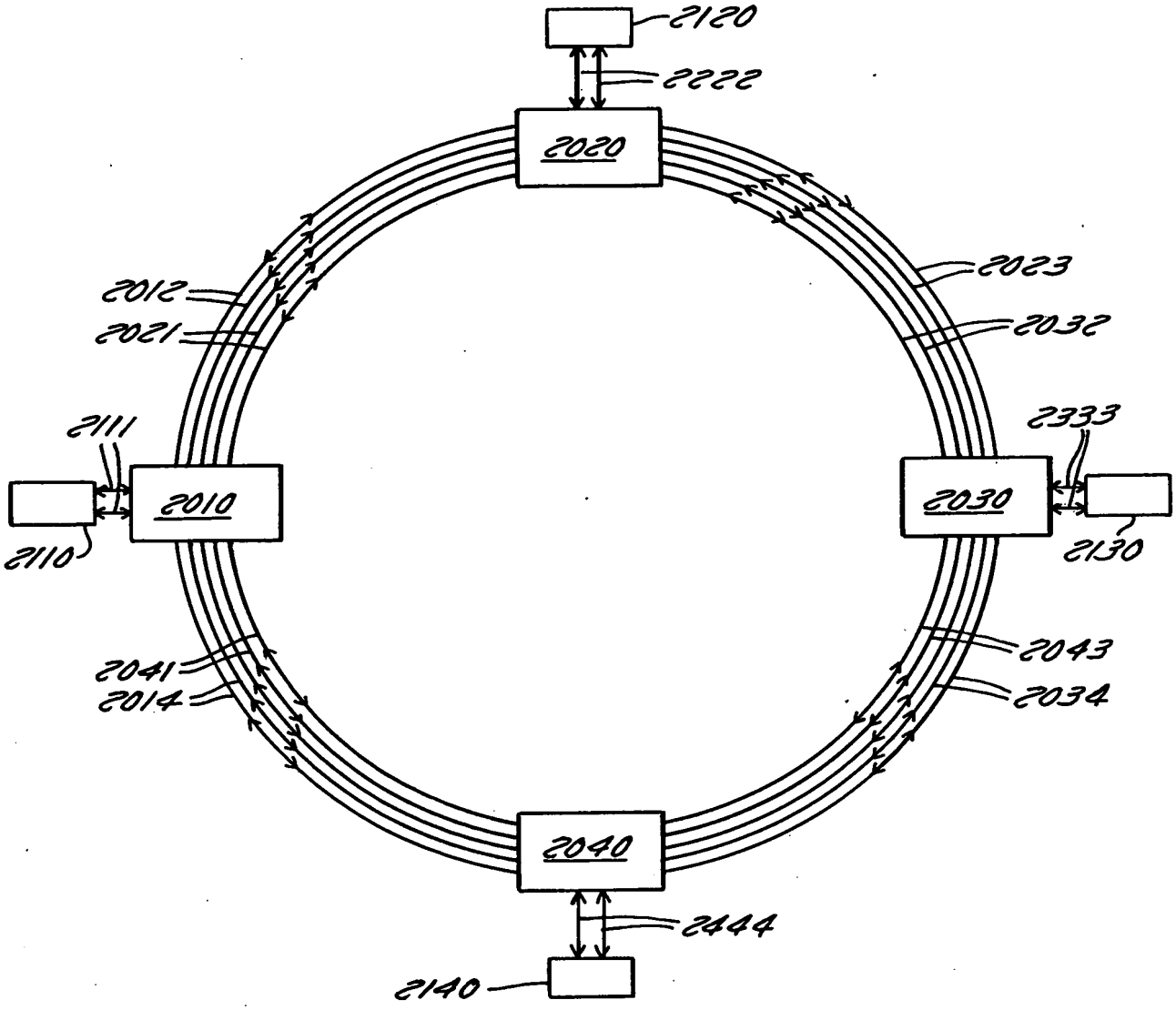
2120
2222
2020
2023
2012
2032
2021
2111
2333
2010
2030
2110
2130
2043
2041
2034
2014
2040
2444
2140

FIG. 14

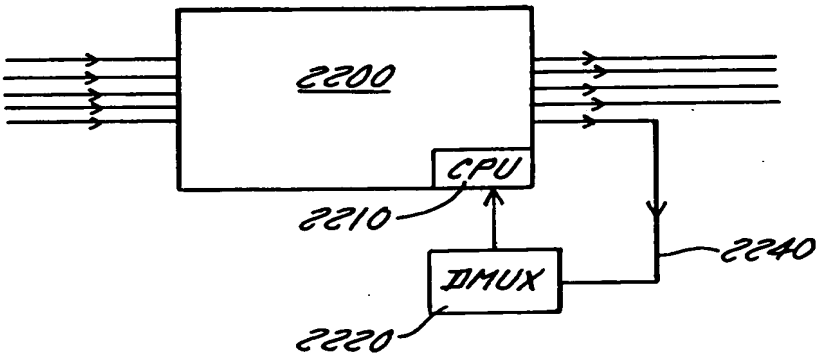
2200
CPU
2210
2240
DMUX
2220

FIG. 15

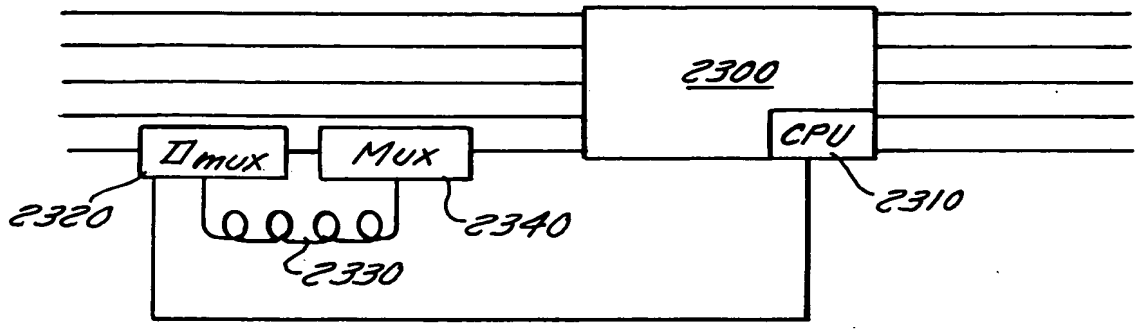
2300
CPU
Dmux
Mux
2320
2340
2330
2310

FIG. 16

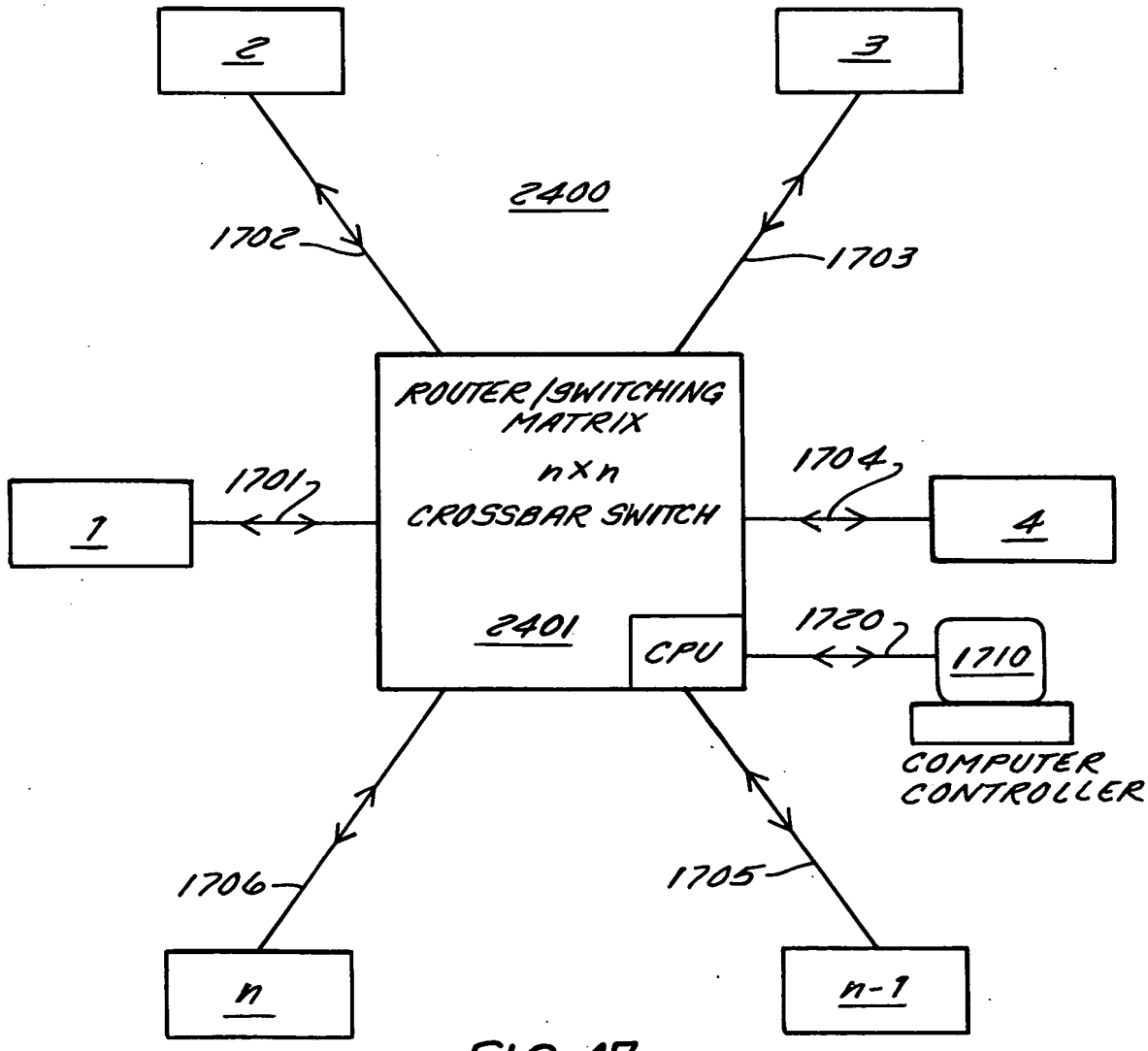
2
3
2400
1702
1703
ROUTER/SWITCHING MATRIX
n x n
CROSSBAR SWITCH
1701
1704
1
4
2401
CPU
1720
1710
COMPUTER CONTROLLER
1706
1705
n
n-1

FIG. 17

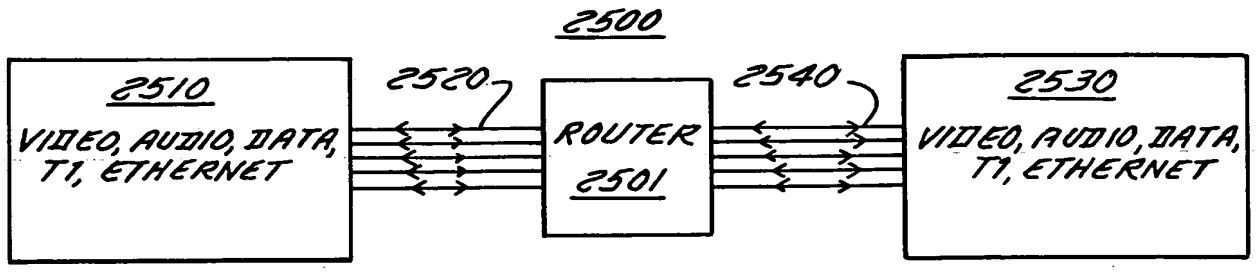
2500
2510
VIDEO, AUDIO, DATA, T1, ETHERNET
2520
ROUTER
2501
2540
2530
VIDEO, AUDIO, DATA, T1, ETHERNET

FIG. 18

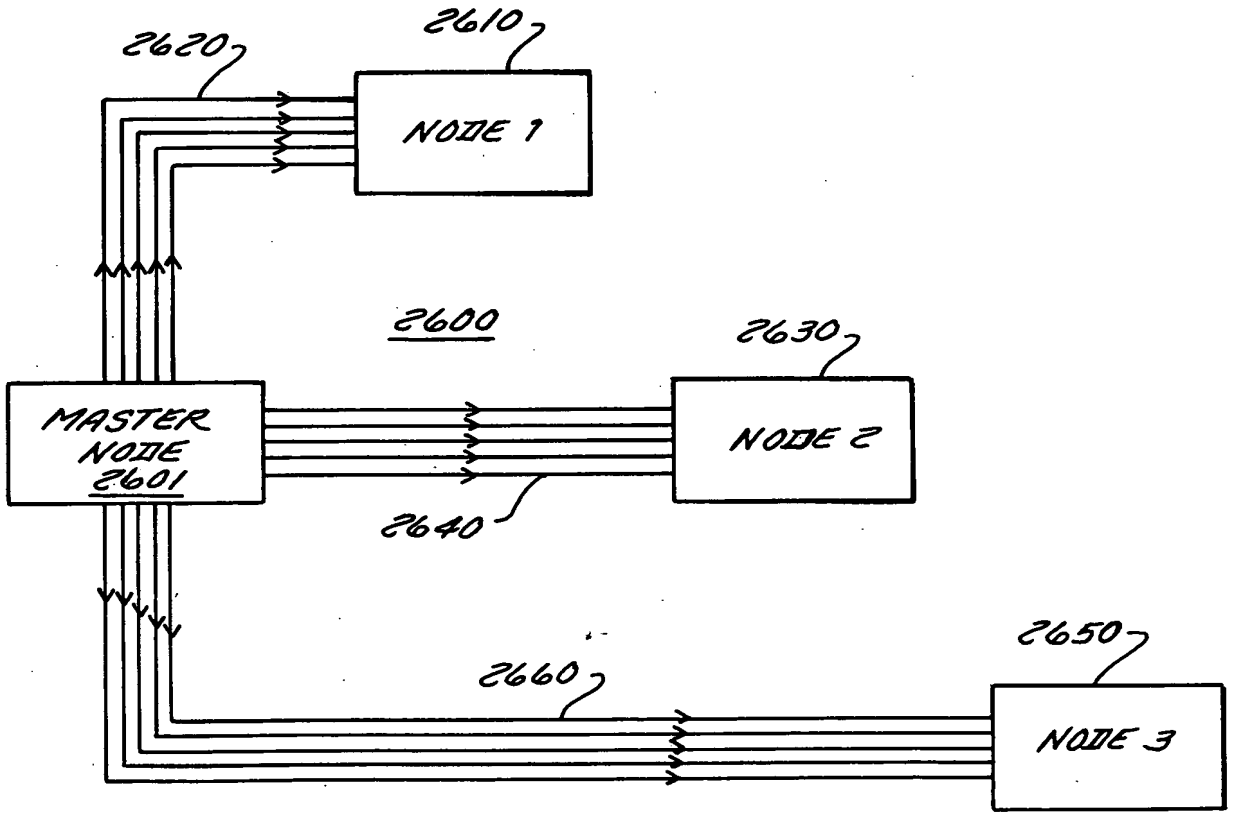
2620
2610
NODE 1
2600
2630
MASTER NODE 2601
NODE 2
2640
2650
2660
NODE 3

FIG. 19

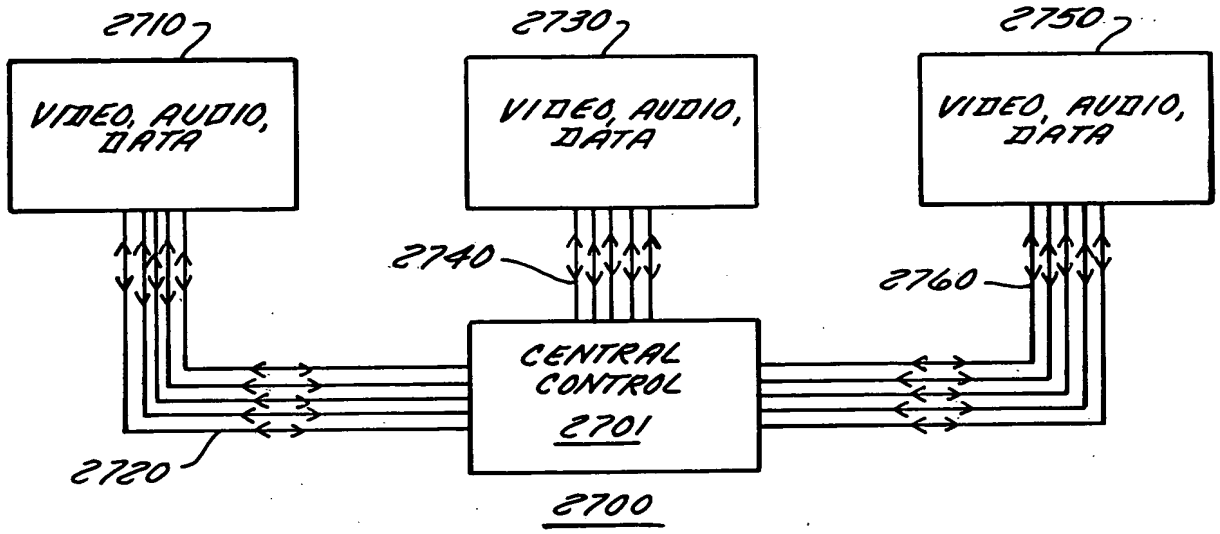
2710
VIDEO, AUDIO, DATA
2730
VIDEO, AUDIO, DATA
2750
VIDEO, AUDIO, DATA
2740
2760
CENTRAL CONTROL
2701
2720
2700

FIG. 20

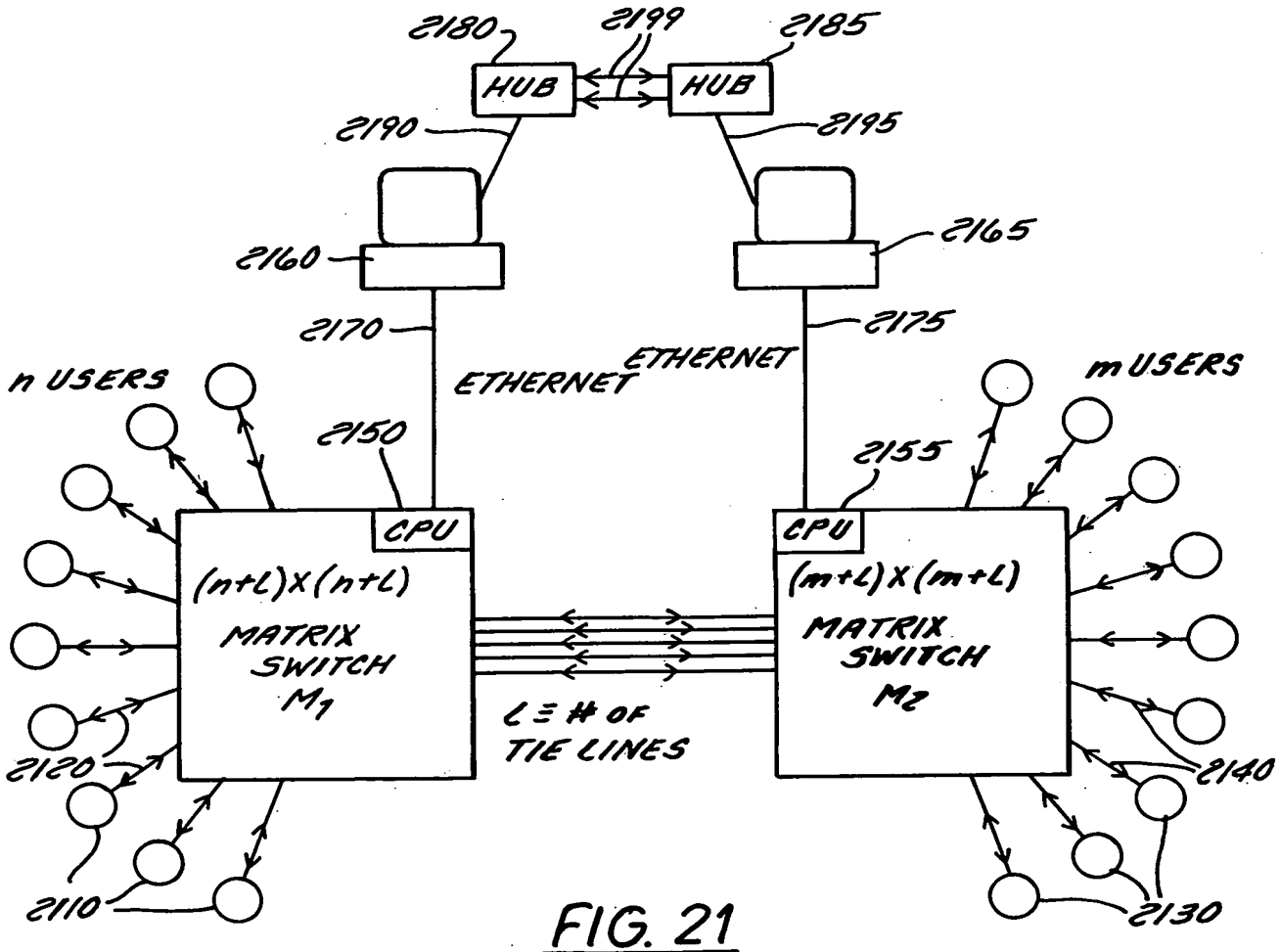
2180
2199
2185
HUB
HUB
2190
2195
2160
2165
2170
2175
ETHERNET
ETHERNET
n USERS
m USERS
2150
2155
CPU
CPU
(n+L)X(n+L)
MATRIX SWITCH M1
(m+L)X(m+L)
MATRIX SWITCH M2
L = # OF TIE LINES
2120
2140
2110
2130

FIG. 21

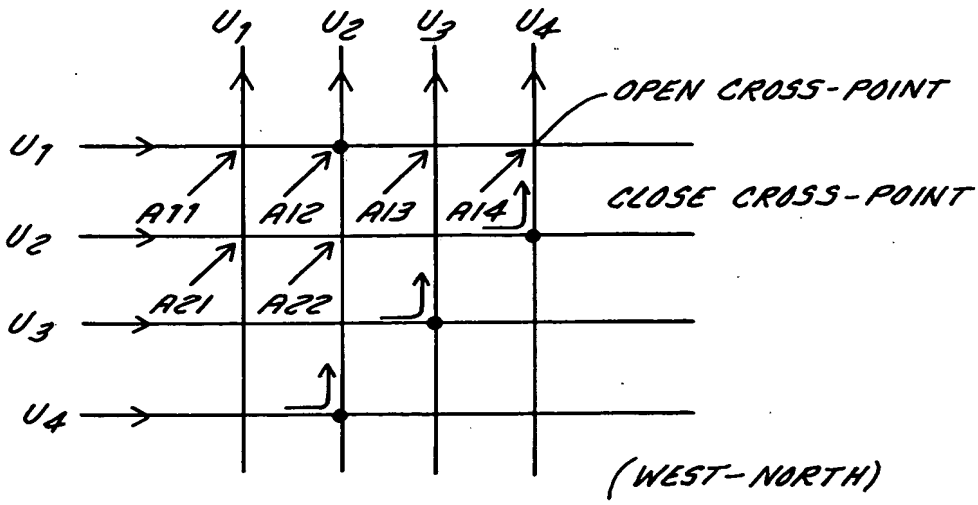
U1
U2
U3
U4
OPEN CROSS-POINT
CLOSE CROSS-POINT
A11
A12
A13
A14
A21
A22
(WEST-NORTH)

FIG. 22

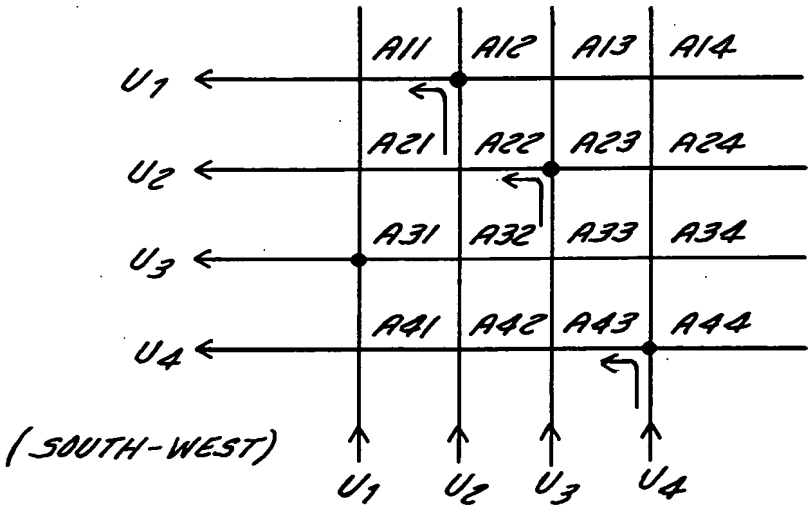
A11
A12
A13
A14
U1
A21
A22
A23
A24
U2
A31
A32
A33
A34
U3
A41
A42
A43
A44
U4
(SOUTH-WEST)
U1
U2
U3
U4

FIG. 23

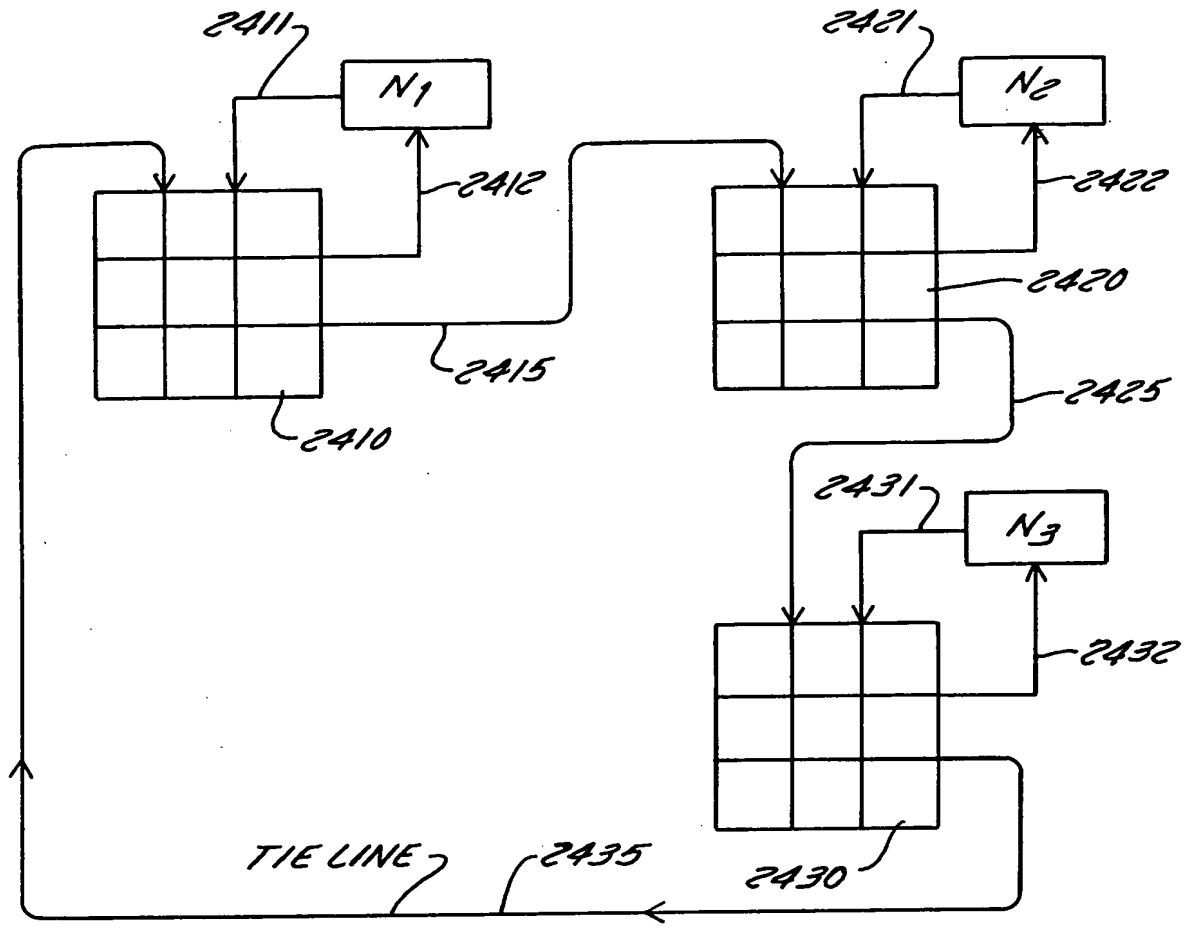
2411
N1
2412
2415
2410
2421
N2
2422
2420
2425
2431
N3
2432
2430
TIE LINE
2435

FIG. 24

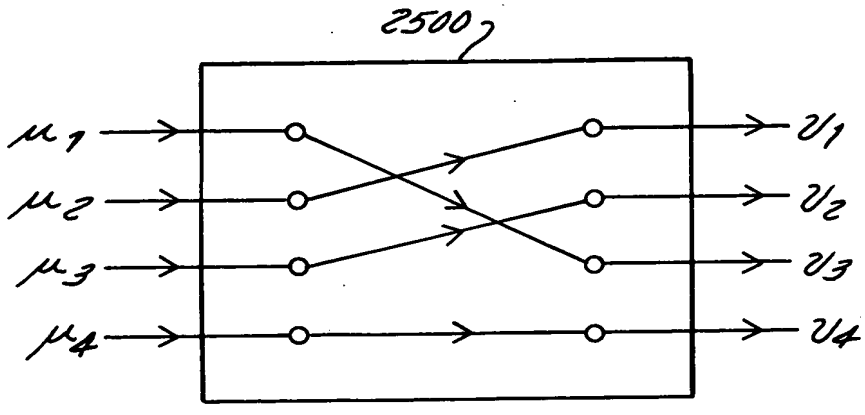
2500
μ1
μ2
μ3
μ4
U1
U2
U3
U4

FIG. 25

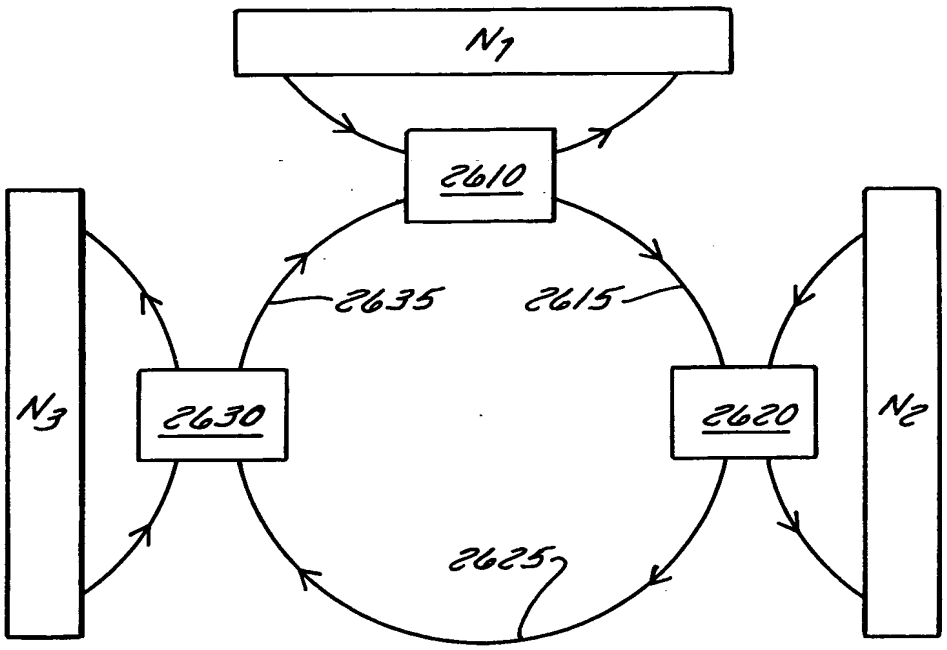
N1
2610
2635
2615
N3
2630
2620
N2
2625

FIG. 26

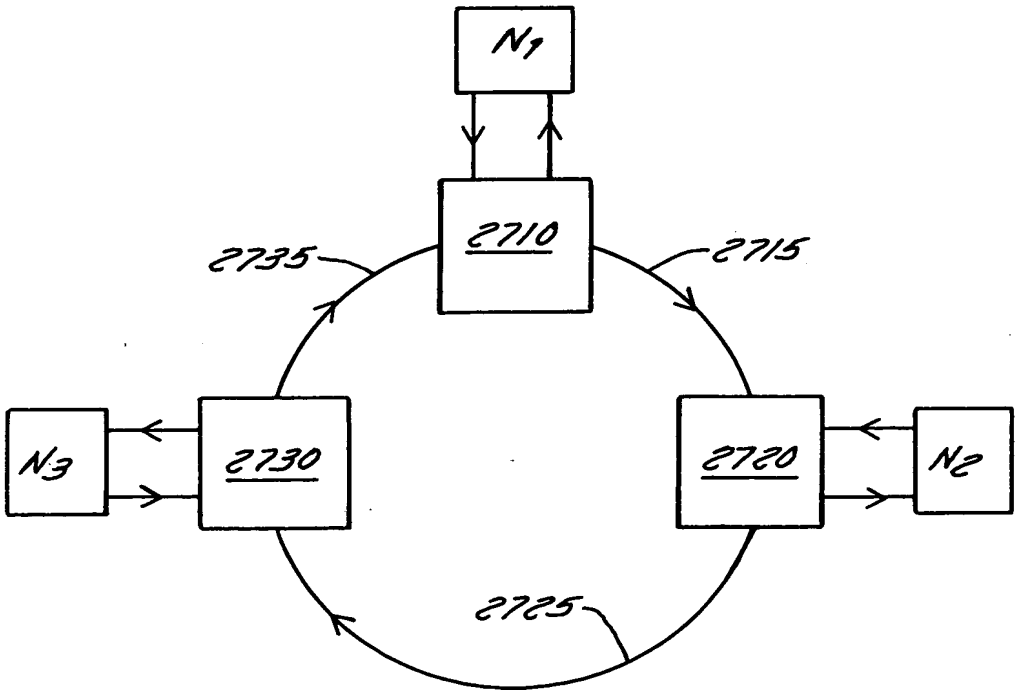
N1
2710
2735
2715
N3
2730
2720
N2
2725

FIG. 27

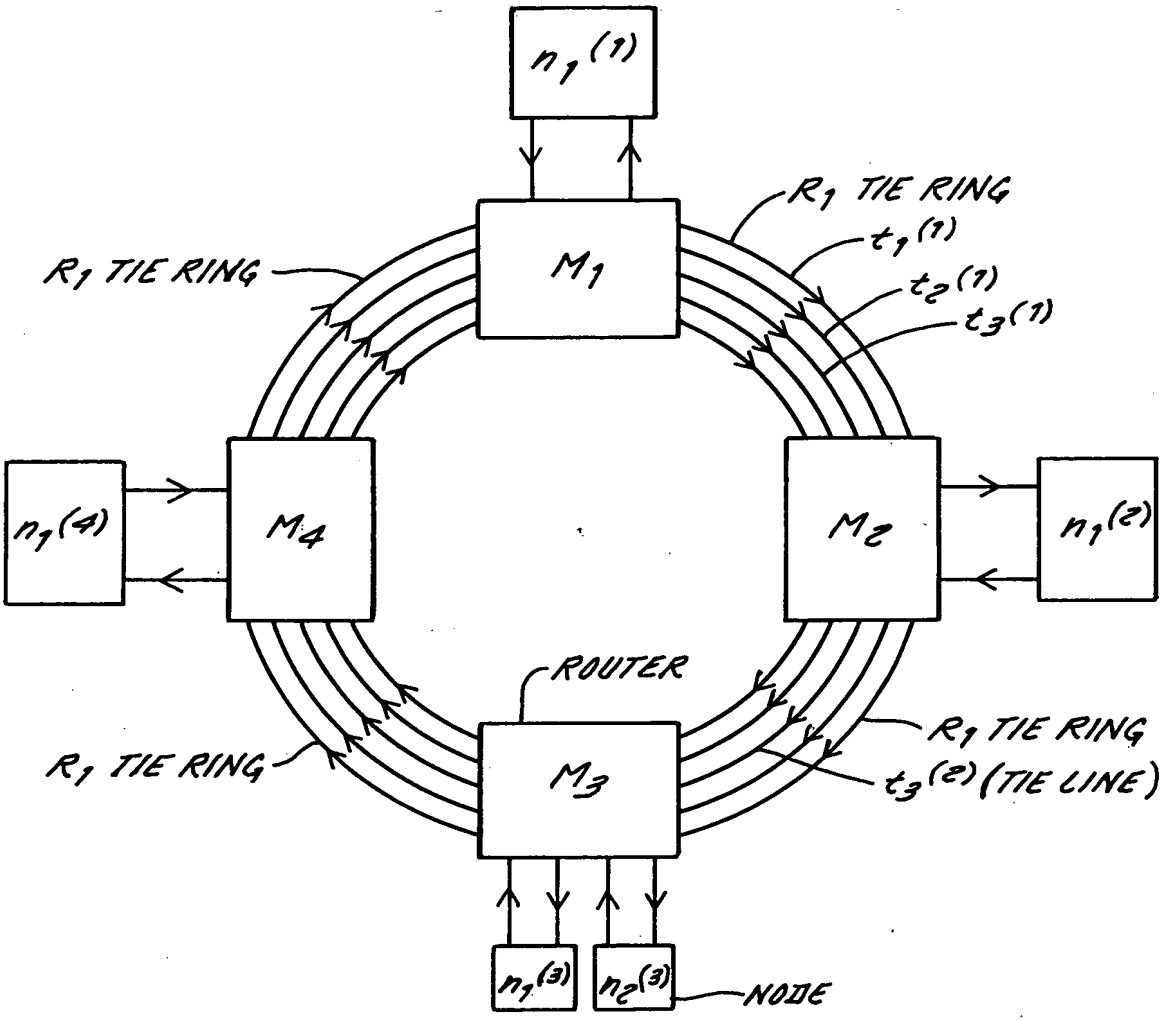
$n_1(1)$
R_1 TIE RING
$t_1(1)$
$t_2(1)$
$t_3(1)$
R_1 TIE RING
M_1
$n_1(4)$
M_4
M_2
$n_1(2)$
ROUTER
R_1 TIE RING
$t_3(2)$ (TIE LINE)
R_1 TIE RING
M_3
$n_1(3)$
$n_2(3)$
NODE

FIG. 28

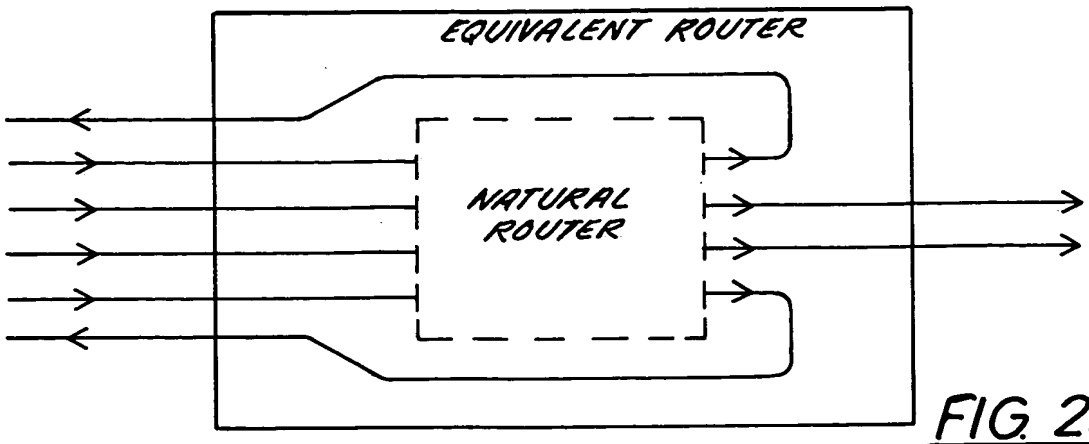

FIG. 29A

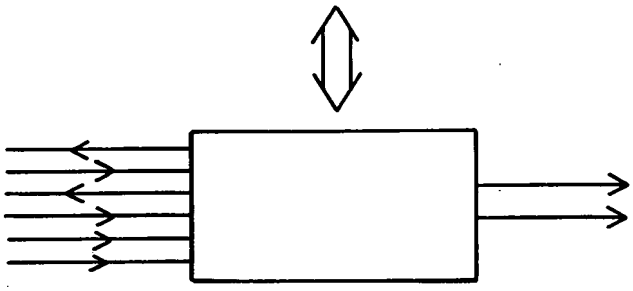

FIG. 29B

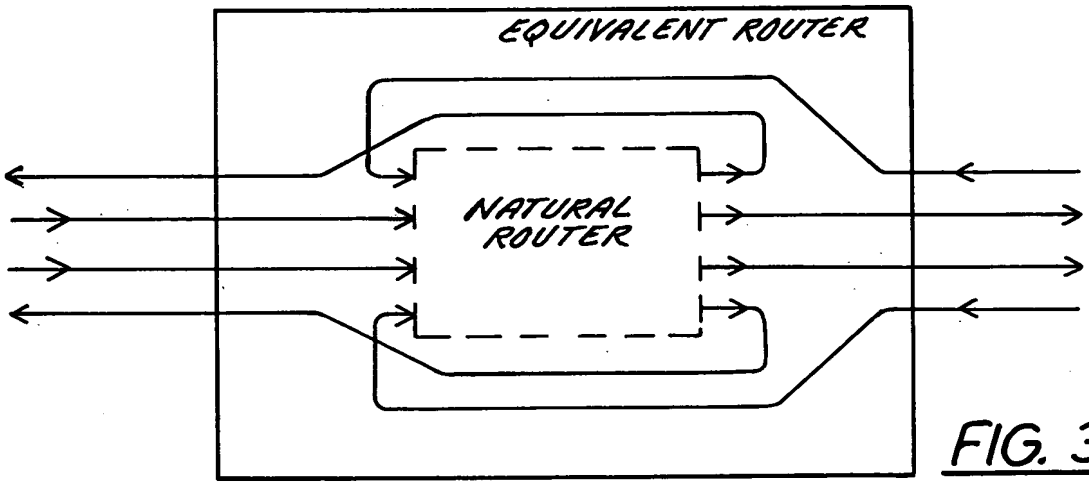

FIG. 30A

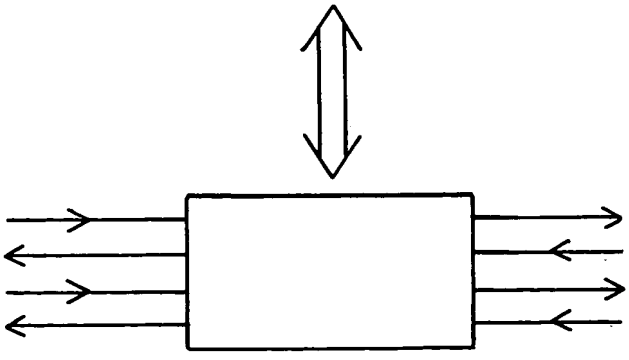

FIG. 30B

09/29/2004

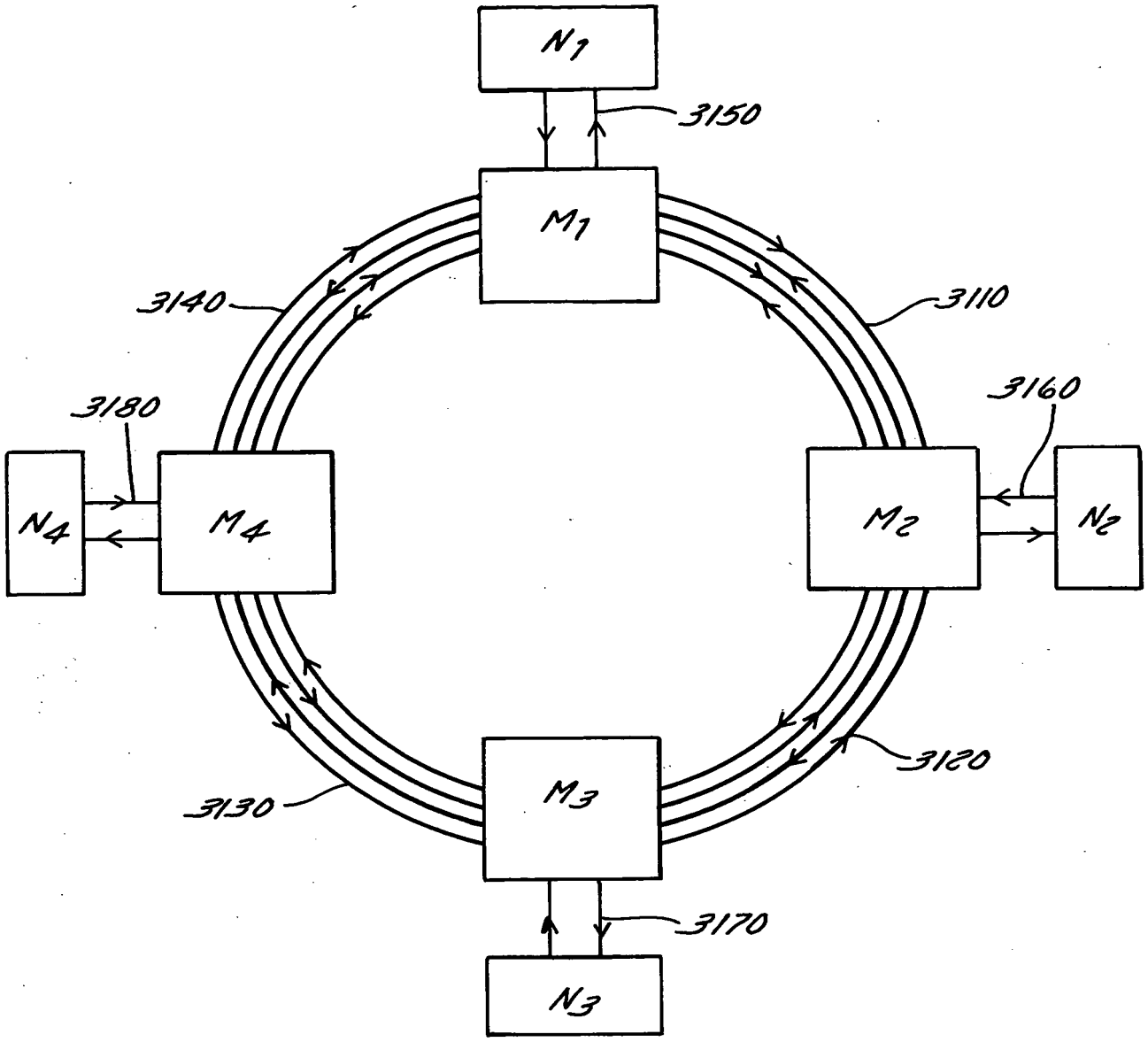

FIG. 31

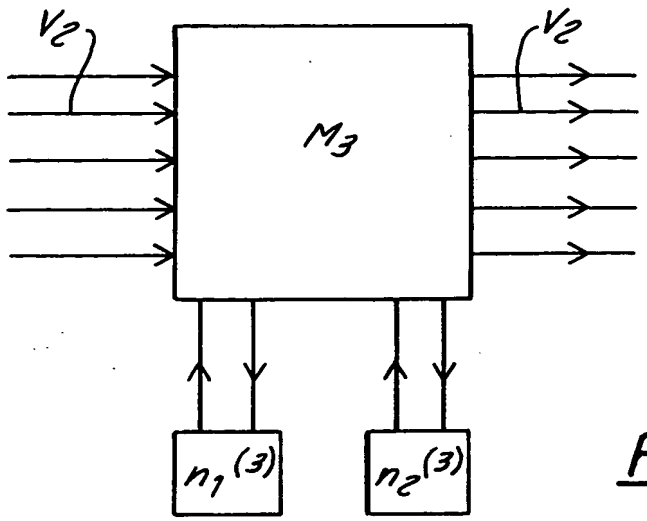

FIG. 32A

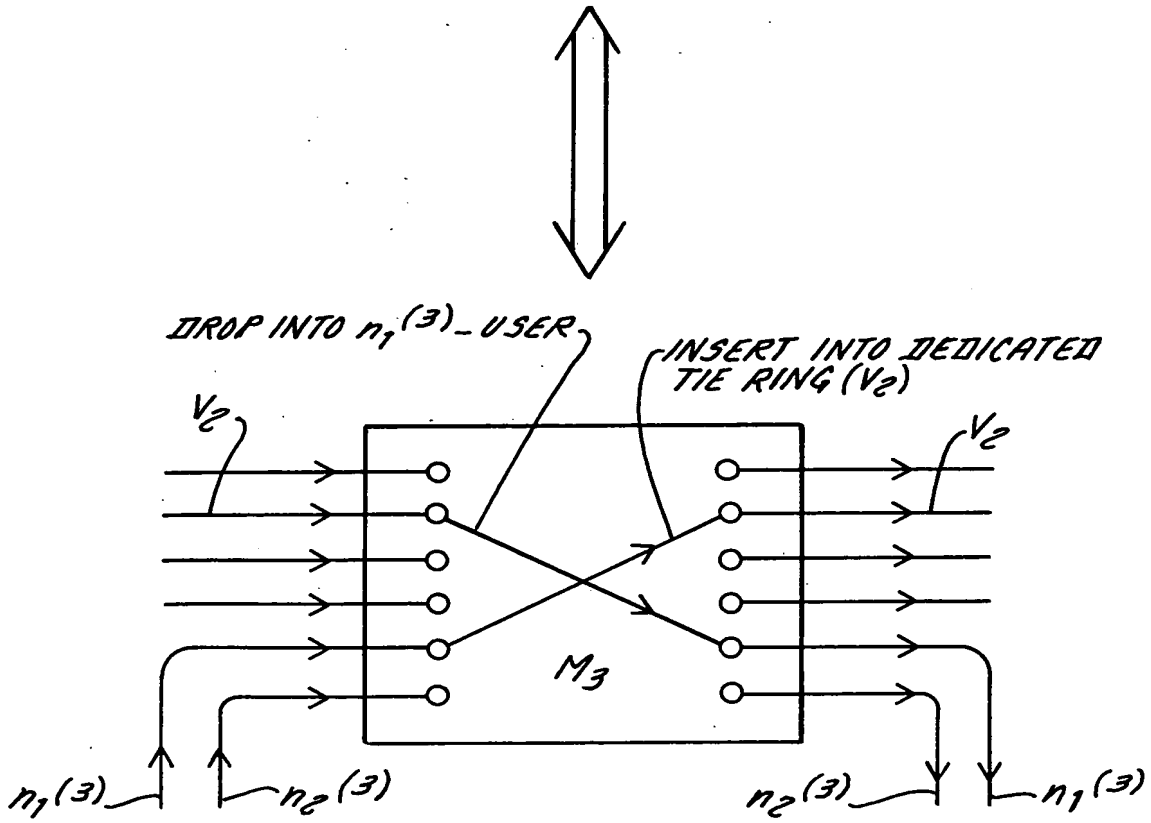

FIG. 32B

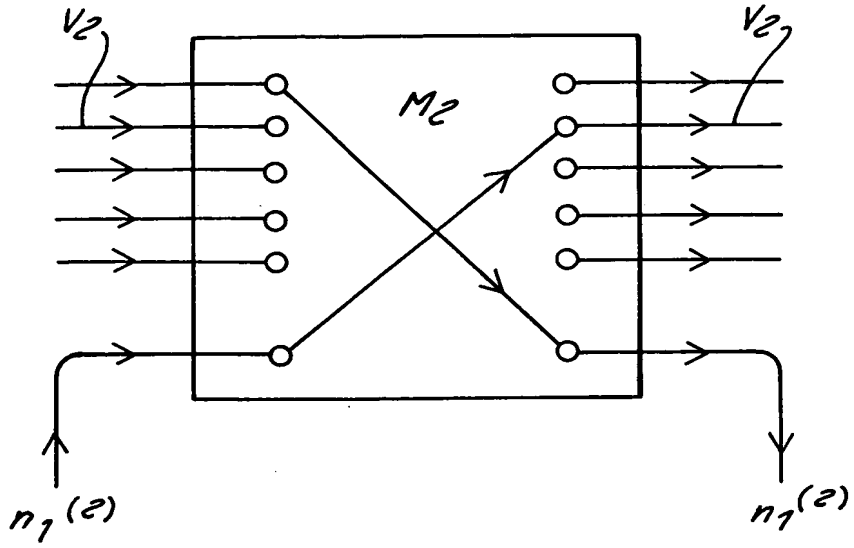

FIG. 32C

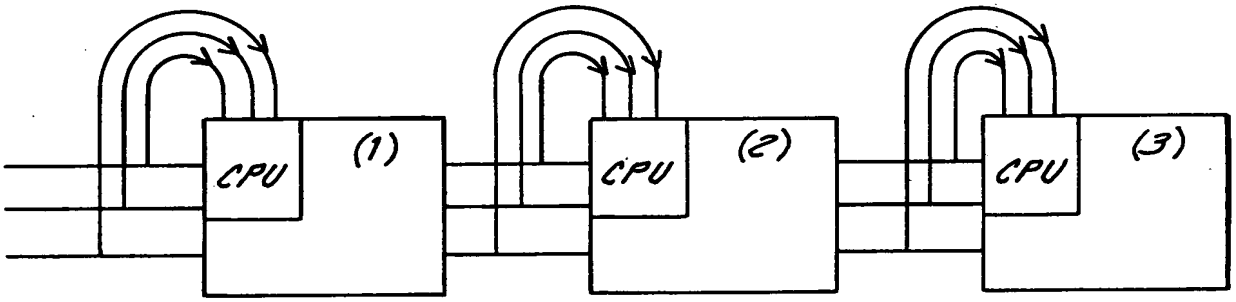

FIG. 32D

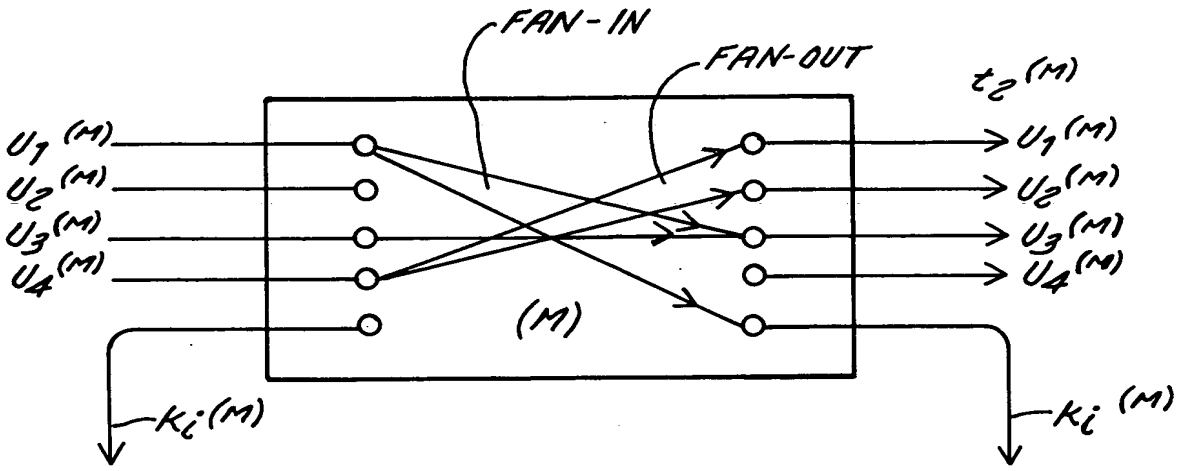
FAN-IN
FAN-OUT
$t_2^{(M)}$
$U_1^{(M)}$
$U_2^{(M)}$
$U_3^{(M)}$
$U_4^{(M)}$
(M)
$K_i^{(M)}$
$K_i^{(M)}$

FIG. 33

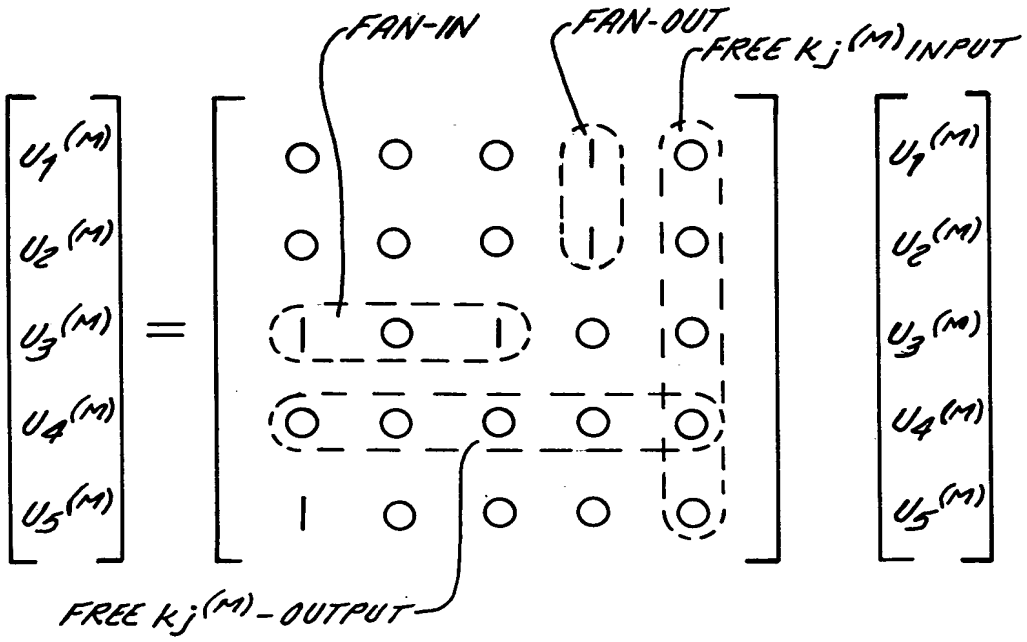
FAN-IN
FAN-OUT
FREE $K_j^{(M)}$ INPUT
$U_1^{(M)}$
$U_2^{(M)}$
$U_3^{(M)}$
$U_4^{(M)}$
$U_5^{(M)}$
=
FREE $K_j^{(M)}$ - OUTPUT

FIG. 34

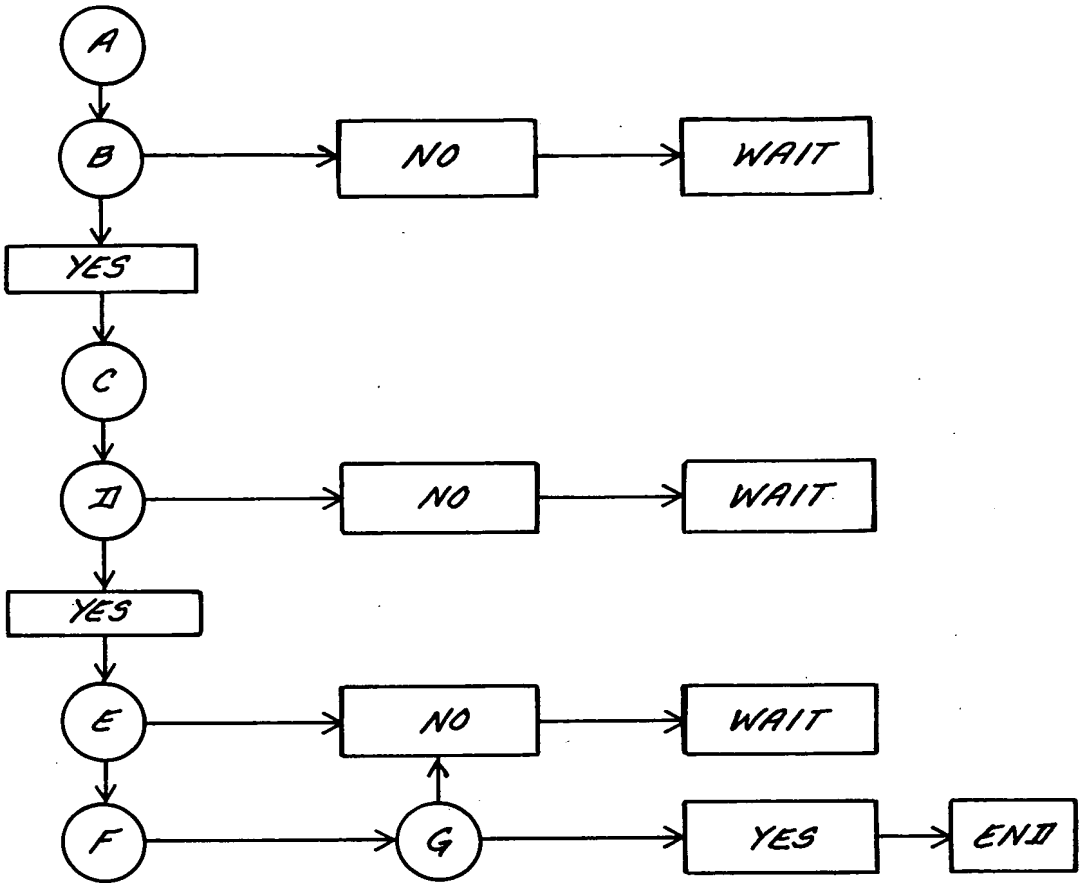
A
B
NO
WAIT
YES
C
D
NO
WAIT
YES
E
NO
WAIT
F
G
YES
END

FIG. 35

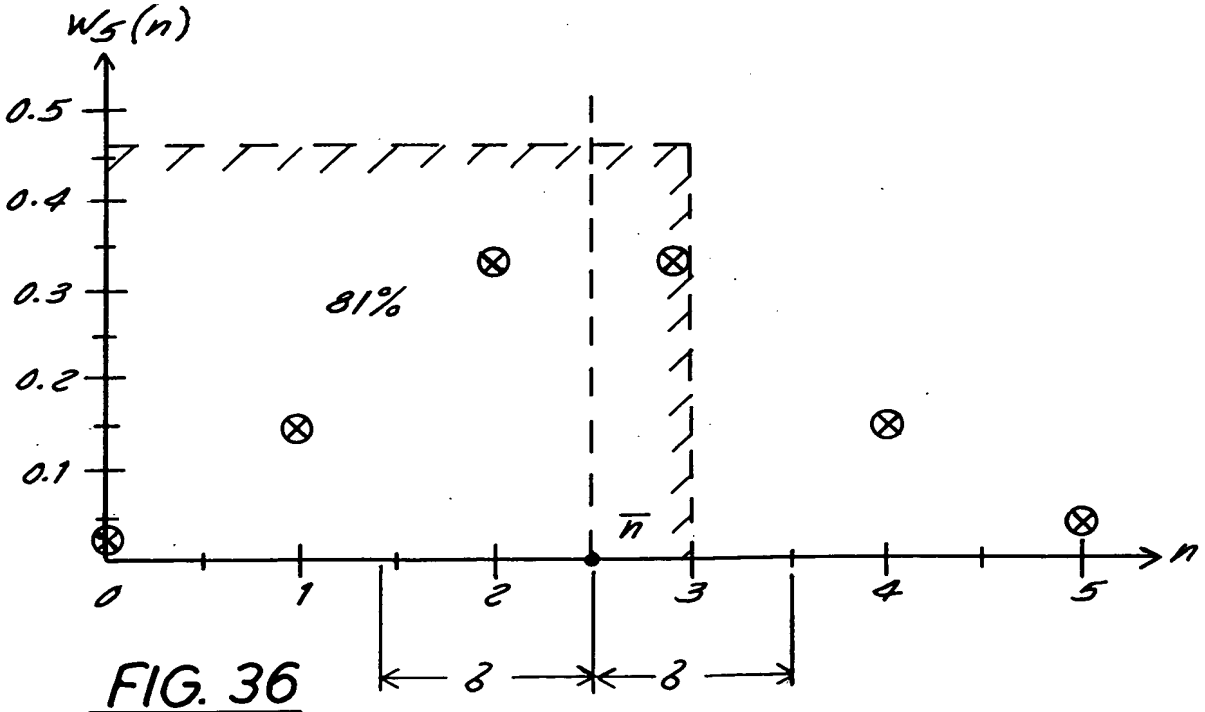
$W_5(n)$
0.5
0.4
0.3
0.2
0.1
81%
$\bar{n}$
0
1
2
3
4
5
n
δ
δ

FIG. 36

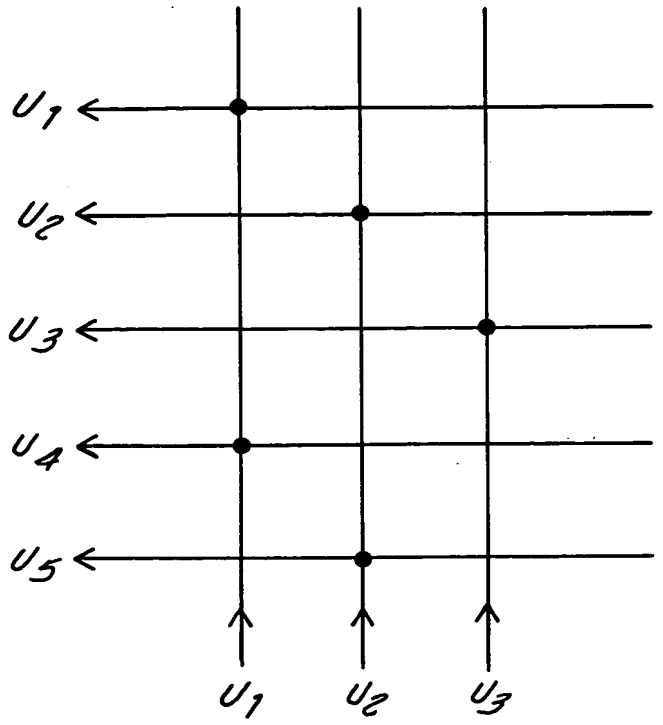

FIG. 37

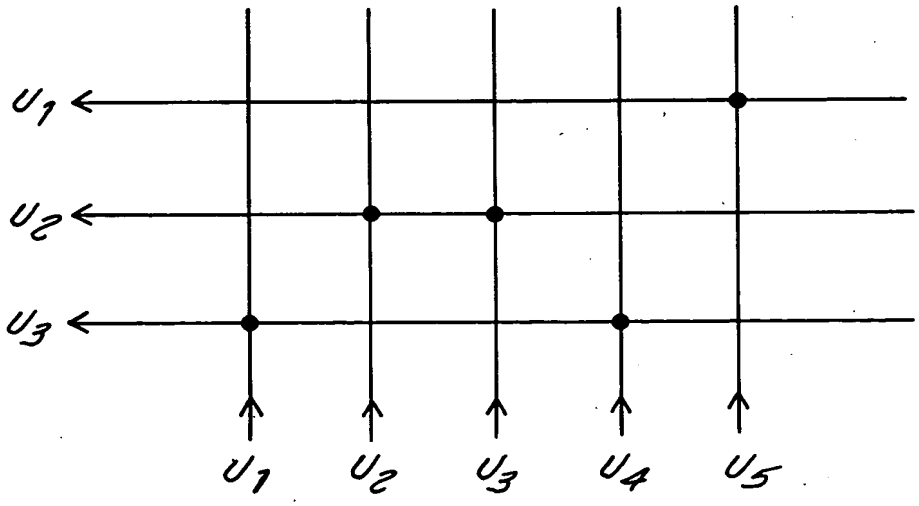

FIG. 38

Approved for Release: 2021/08/04 C05102574

T09020-0262260

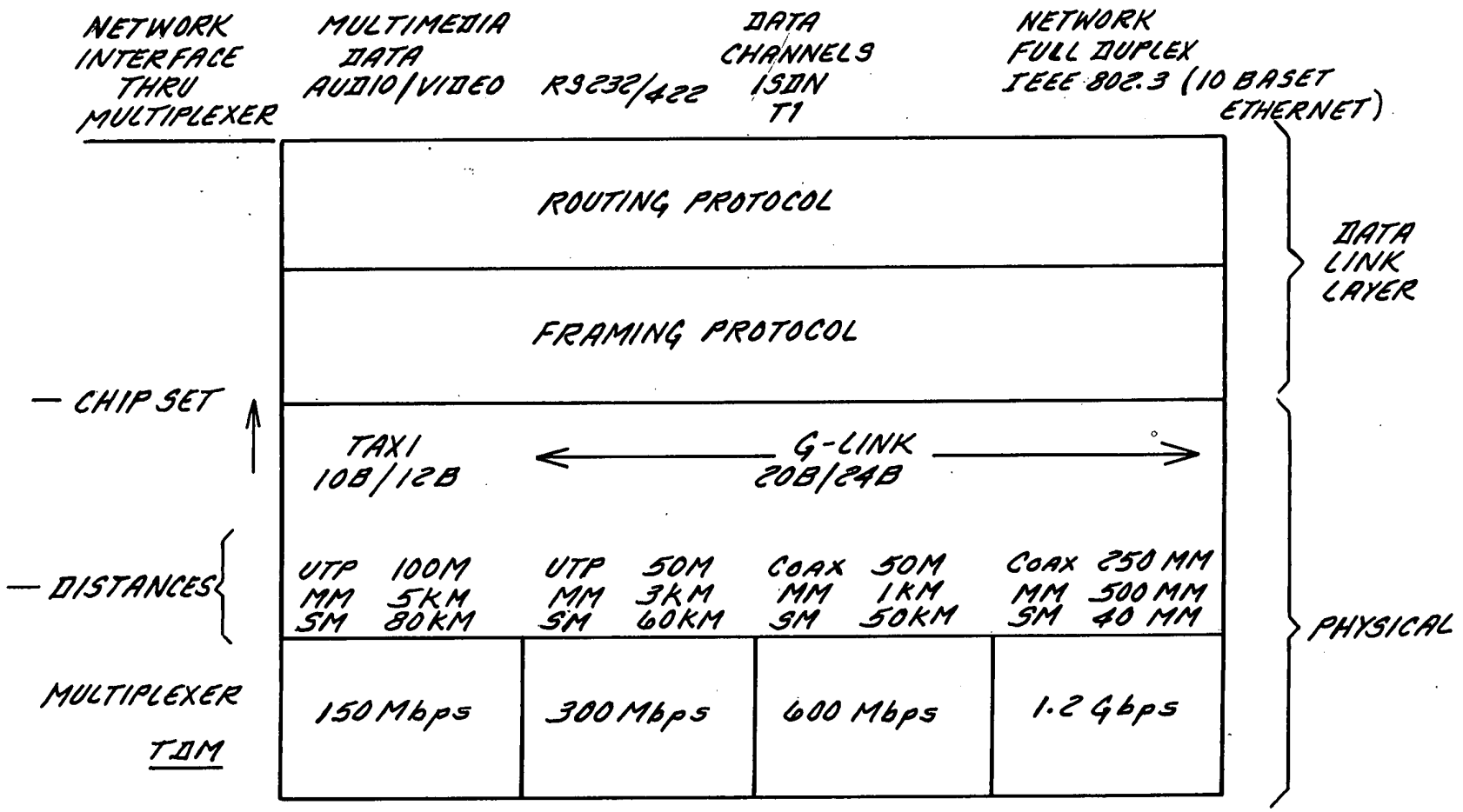

FIG. 39

T09020"02627760

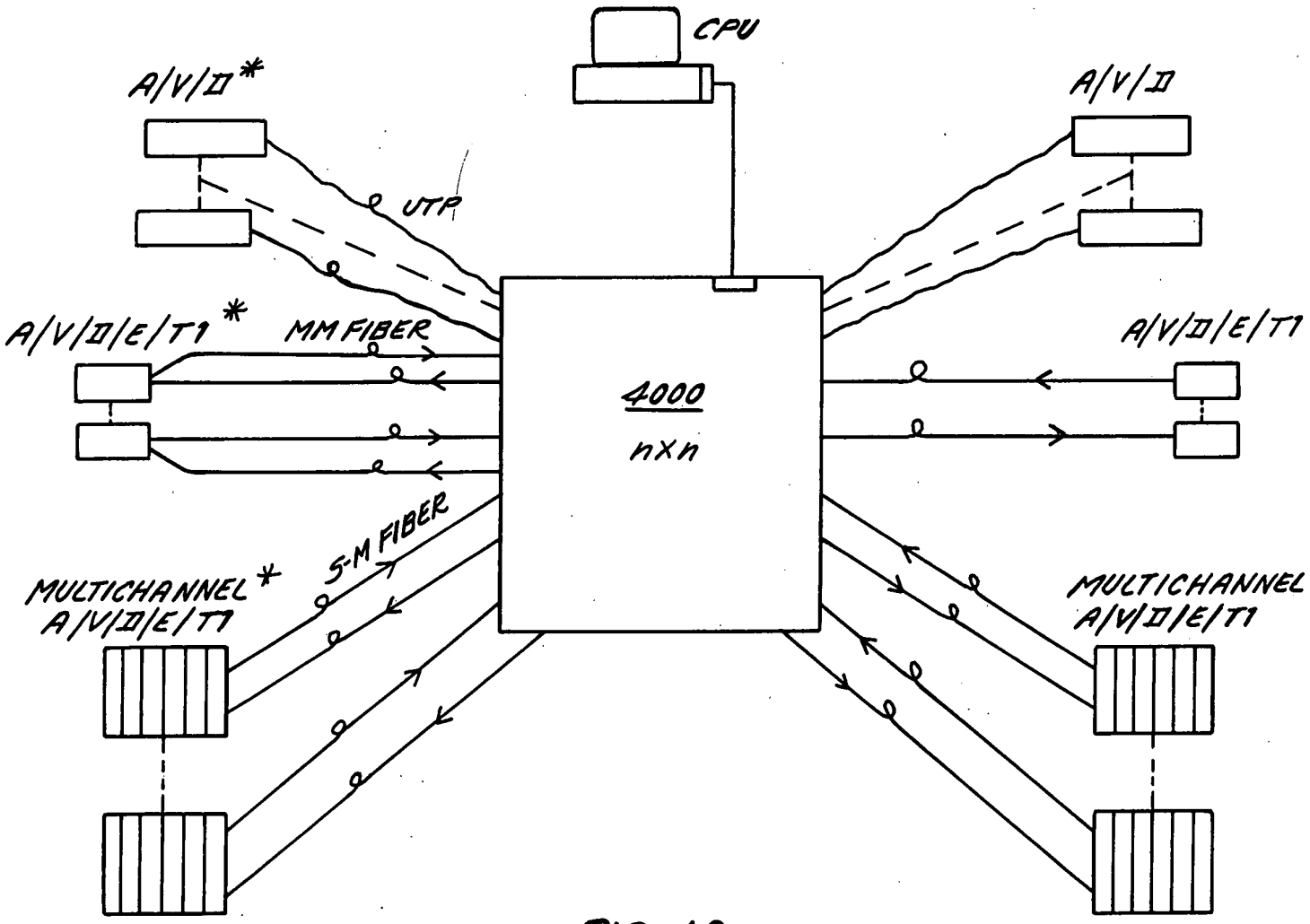

FIG. 40

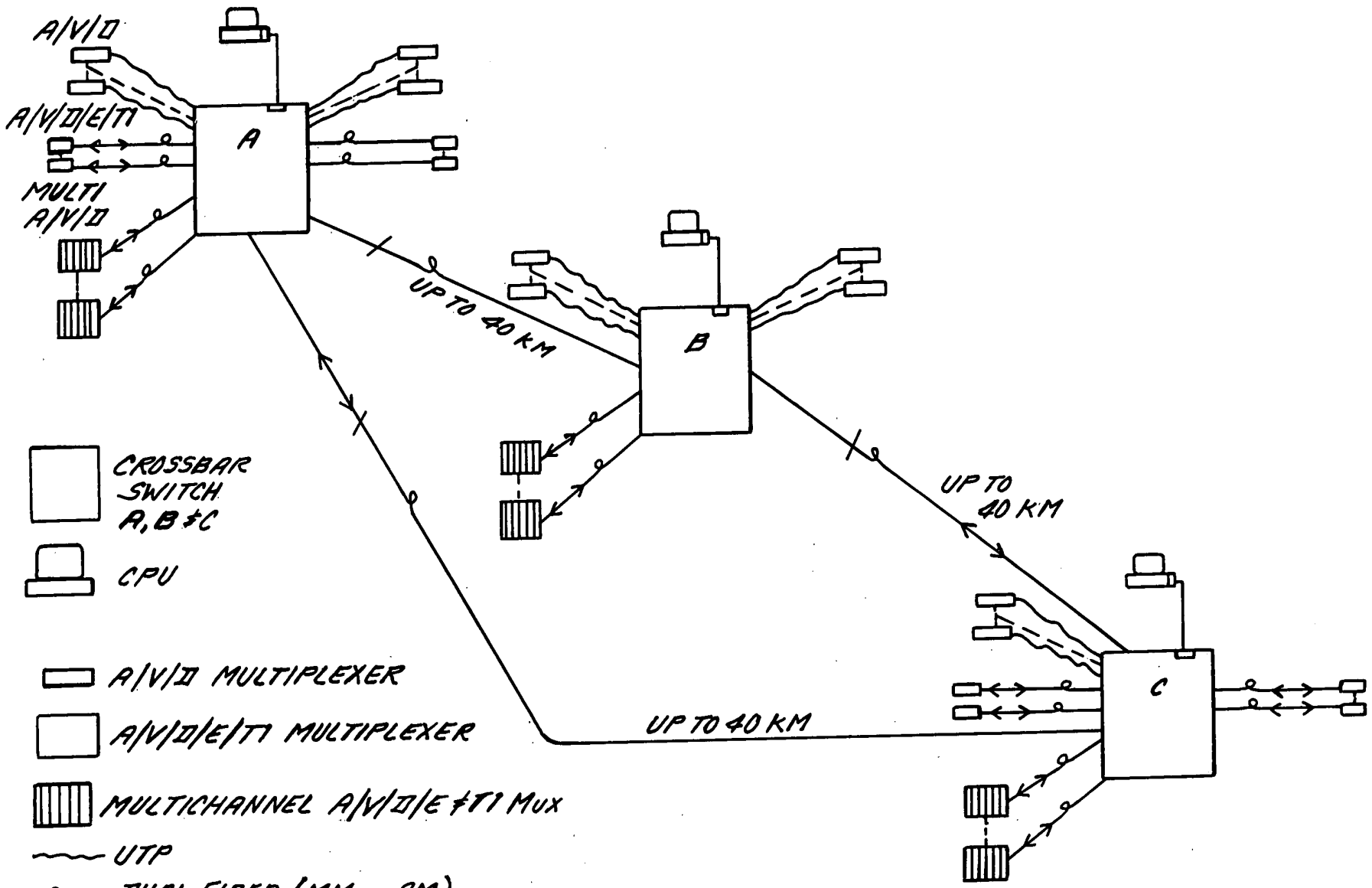
A/V/D
A/V/D/E/T1
MULTI A/V/D
A
B
C
UP TO 40 KM
UP TO 40 KM
UP TO 40 KM
CROSSBAR SWITCH A, B & C
CPU
A/V/D MULTIPLEXER
A/V/D/E/T1 MULTIPLEXER
MULTICHANNEL A/V/D/E & T1 MUX
UTP
DUAL FIBER (MM OR SM)
FIBER BUNDLE

FIG. 41

T09020" 09727970

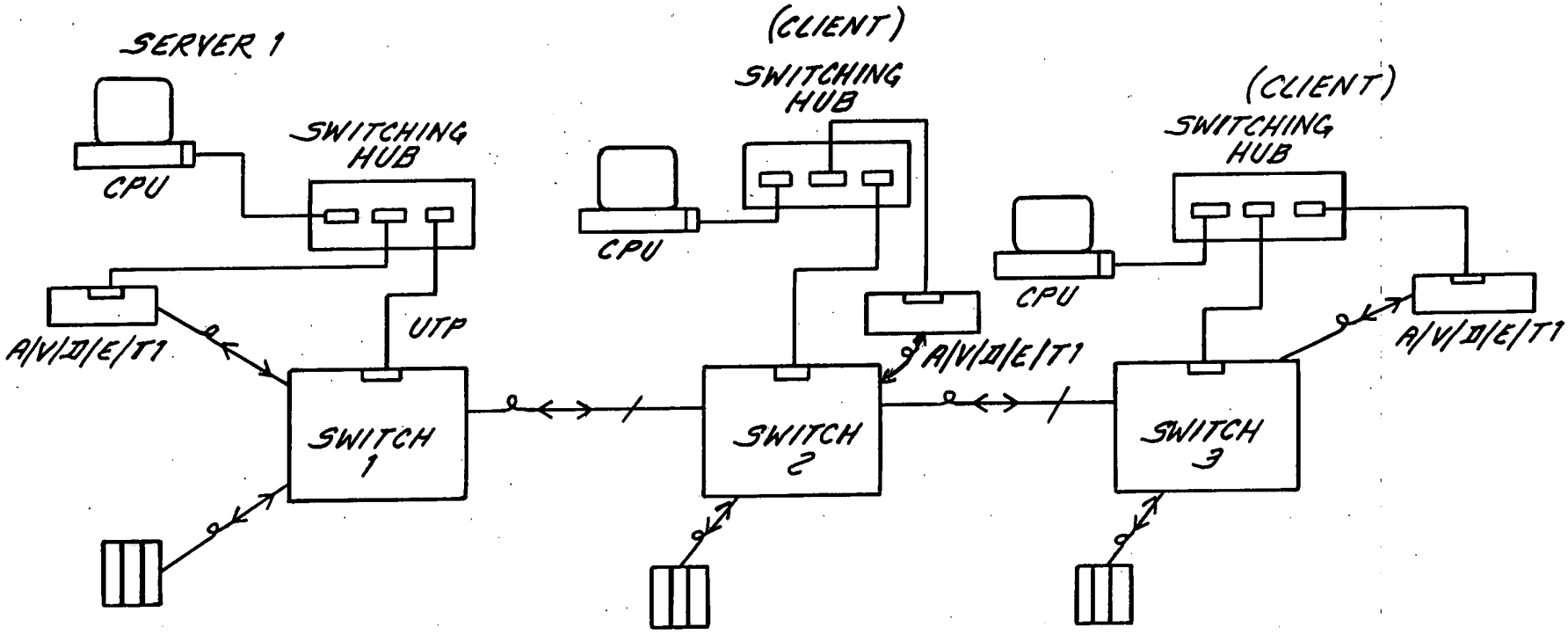

FIG. 42

T09020' 02677260

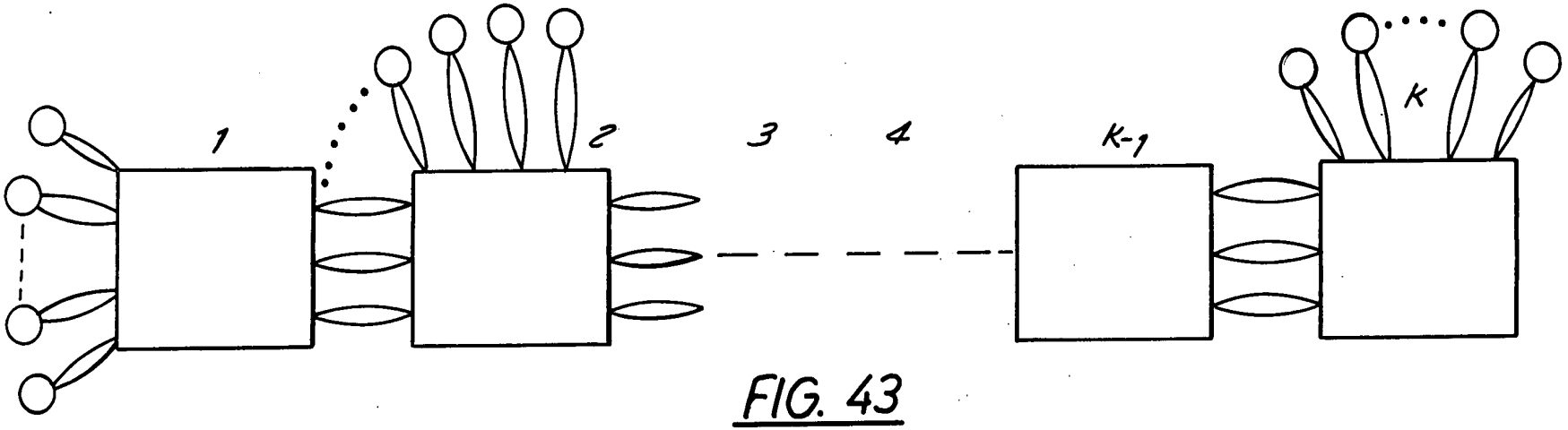

FIG. 43

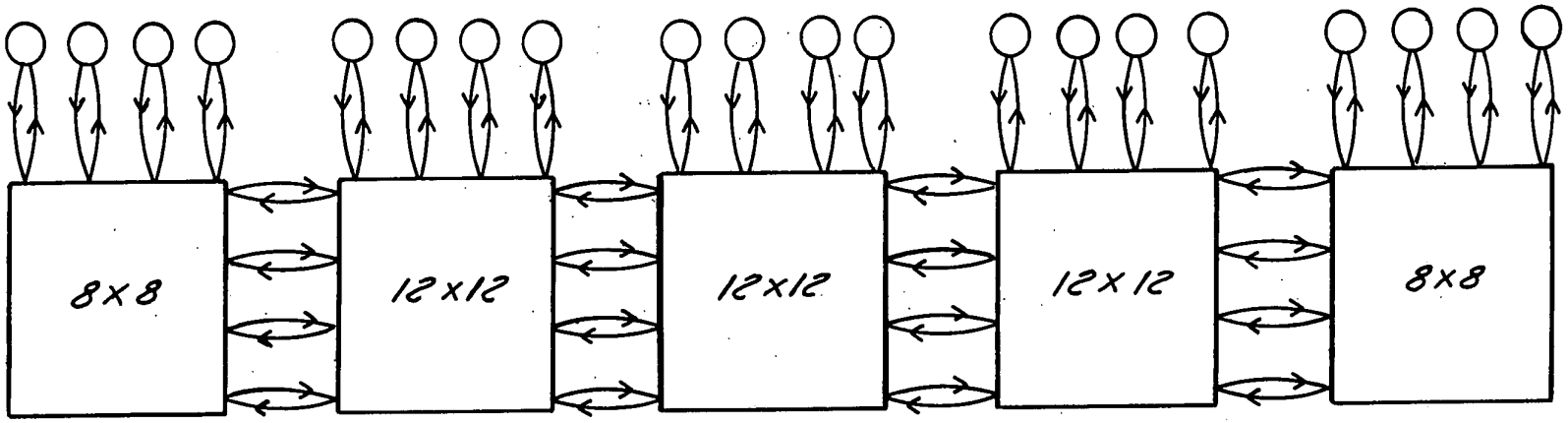

FIG. 44

T09020" 02677760

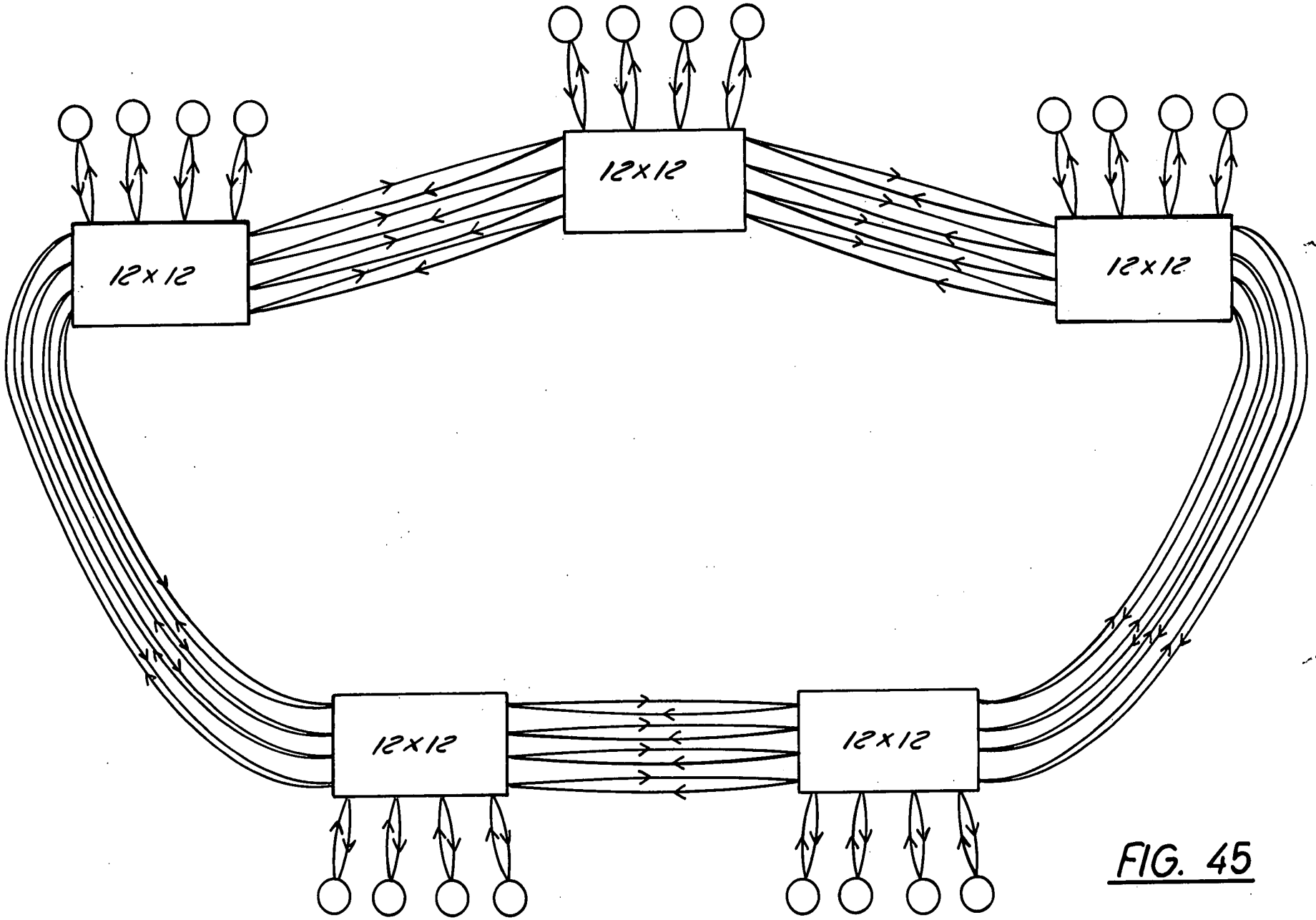

FIG. 45

T09020" 0267260

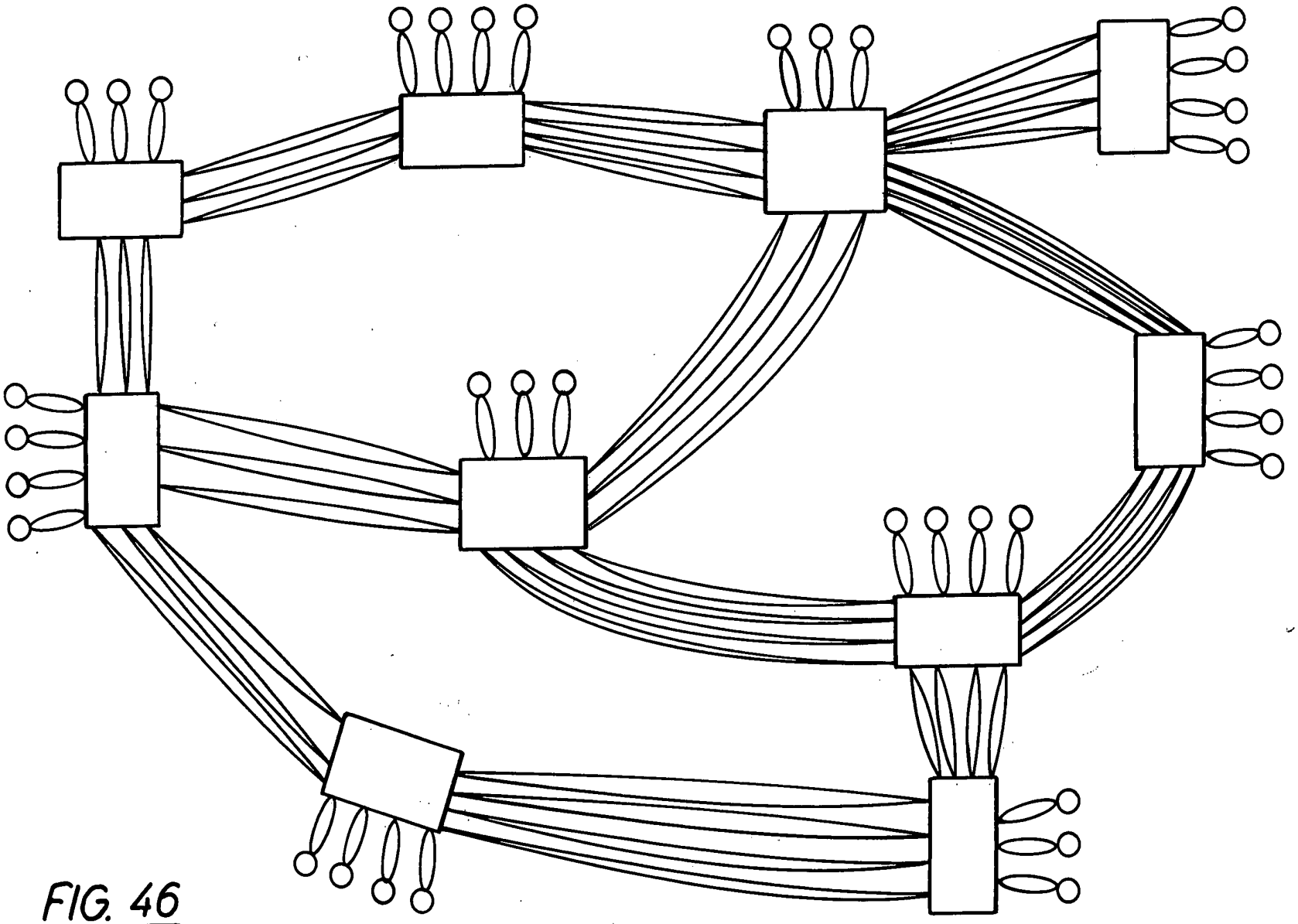

FIG. 46